Electromagnetic Compatibility of Integrated Circuits
Advances and Issues

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Summary

I. Past
II. Present
III. Evolution of ICs and consequence on EMC
IV. Measurement of IC emission and susceptibility
V. Models for EMC simulation
VI. Design Rules for Improved EMC and signal integrity
VII. Future - What is next?
I. Past

43 years ago…

Air Force Weapon Laboratory, USA

SPECTRE

- Effects of the electromagnetic fields triggered by nuclear explosions on electronic devices used in missile launch sites.
- Simulation software developed at IBM (Sedore, 1965)
- Correlate simulations and experimental measurements obtained on an electromagnetic impulse test-bench.
29 years ago…
IEEE Trans on EMC, 1979
Special issue on RF interference in ICs

- Rising risk of interference between ICs and electromagnetic sources
- Very High Frequency (30 MHz - 300 MHz)
- Visionary editorial about future problems due to higher speed and integration

14 years ago…
IEEE Trans on Power Electronics, 1994
Emission reduction techniques (F. Lin)

(Virginia Polytechnic Institute, USA)
10 years ago…
IEEE Trans on EMC, 1998
Technology Comparisons (M.P. Robinson)

Robinson (Univ. York) compared the radiated emissions produced by different families of logic circuits. Significant behavioral differences were observed.

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9 years ago…
First workshop dedicated to EMC of ICs (1999)

…and the next events (approx each 18 months)
2 years ago...

“EMC of ICs”, Springer, USA, 2006

Ben Dhia, Ramdani and Sicard compile the first book only dealing with EMC at integrated circuit level. The book includes a description of measurement, model standards, techniques for low emission and susceptibility.

II. Present
Industrial pressure

Susceptibility

- Carbon airplane
- Equipment
- Boards
- Radar
- Components

Emission

- Personal entrainments
- Mobile phone
- Safety systems
- Control systems

System EMC impacts ICs

Emission and immunity levels (dB)

- Security margin
- Small margin
- Immunity
- Interference risk

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Why a margin

Acceptable emission level
- Security
- Process variations
- Measurement error
- Ageing
- Environnement

Margin depends on application

<table>
<thead>
<tr>
<th>Domain</th>
<th>Life time</th>
<th>Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Automotive</td>
<td>15 years</td>
<td>20 dB</td>
</tr>
<tr>
<td>Mobile phone</td>
<td>1 year</td>
<td>0 dB</td>
</tr>
<tr>
<td>Aeronautics</td>
<td>30 years</td>
<td>40 dB</td>
</tr>
</tbody>
</table>

Low emission = differentiator

Low parasitic emission has become a key commercial argument

Customer's specified limit

EMC compliant

Not EMC compliant
Main interest: 10 MHz – 3 GHz

Parasitic emission (dB)

Frequency

The IC as an antenna

Frequency

Band

Wave length

Smith Chart

Wireless systems
III. Evolution of IC technology and consequence on EMC

Progresses in Lithography

- 80286 Submicron
- 80386 Deep Submicron
- Pentium II 200MHz
- Pentium III 1.0GHz
- Pentium, IV 3.0GHz
- Core2 65nm
- Xeon 45nm
- 32nm
- 22nm
- Working at 0.5nm

What my teachers said (1980)
What I said to my students (1990)
Increased Complexity

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.18µm</th>
<th>0.12µm</th>
<th>90nm</th>
<th>65nm</th>
<th>45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complexity</td>
<td>50M</td>
<td>100M</td>
<td>250M</td>
<td>500M</td>
<td>1G</td>
</tr>
<tr>
<td>Packaging</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**IC example**

<table>
<thead>
<tr>
<th>Current peak</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>µC 16b</strong> 0.5 A</td>
</tr>
<tr>
<td><strong>µC</strong> 2 A</td>
</tr>
<tr>
<td><strong>µC+DSP</strong> 10 A</td>
</tr>
<tr>
<td><strong>µC+DSP Flash Ram</strong> 30 A</td>
</tr>
<tr>
<td><strong>Multicore, DSP, FPGA, RF</strong> 100 A</td>
</tr>
</tbody>
</table>

Consequence on Emission

Basic inverter switching (50 % of the core)

45 nm: Current: 0.1mA/gate, 100 million of gates

10,000 Amp peak
Increased switching noise

Why technology progresses make things worse

- The current amplitude is a little reduced
- The switching is faster

Wider Noise Spectrum

Internal current peaks in integrated circuits produce the highest amount of harmonics

Amplitude (A) Fourier

50ps

Time

Clock 1 GHz, rise time 50 ps
Susceptibility Issues

Less voltage margin

Supply (V)

- 5.0
- 3.3
- 2.5
- 1.8
- 1.2
- 0.7

Technology

0.5μ 0.35μ 0.18μ 90nm 65nm 45nm

150 mV margin

I/O supply

Core supply

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Impact on Design Cycle

EMC problems handled at the end of design cycle: 3rd cause of redesign

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EMC-aware Design Cycle

**DESIGN**
- Architectural Design
- Design Entry
- Design Architecture

**Tools**
- Design Guidelines
- Training

**EMC Simulations**
- Compliance ?
  - GO
  - NO GO

**FABRICATION**
- EMC compliant

EMC validated **before** fabrication

IV. Measurement of IC
Emission & Susceptibility

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The Formal side of IEC

47A/786/NP
NEW WORK ITEM PROPOSAL

Proposer: United States

WG/SC: SC 47A

Date of proposal: 2004-03

Date of circulation: 2004-03-14

 WG 2 : Digital integrated circuits
 WG 9 : Test procedures and measurement methods for EMC of ICs

  Members
  § USA
  § Japan
  § South Korea
  § Germany
  § France
  § Poland
  § Italy
  § England
  § Netherlands

47A.2.151 E1 [A0-1]

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### Measurement of Emission

Standard Measurement methods exist, some are limited to 1 GHz

<table>
<thead>
<tr>
<th>Method</th>
<th>Description</th>
<th>Frequency Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEC 61967-2</td>
<td>TEM : 1GHz</td>
<td>1 GHz</td>
</tr>
<tr>
<td>IEC 61967-3/6</td>
<td>Near-field Scan, 5GHz</td>
<td>1 GHz</td>
</tr>
<tr>
<td>IEC 61967-4</td>
<td>1/150 ohm, 1 GHz</td>
<td>1 GHz</td>
</tr>
<tr>
<td>IEC 61967-8</td>
<td>Mini-stripline</td>
<td></td>
</tr>
<tr>
<td>IEC 61967-7</td>
<td>Mode Stirred Chamber : 18 GHz</td>
<td></td>
</tr>
<tr>
<td>Ext: IEC 61967-2</td>
<td>GTEM 18 GHz</td>
<td></td>
</tr>
</tbody>
</table>
A Zoom on Near-field Scan

Small Magnetic probe (IEC 61967-3)

Time-domain Near Field

Time-domain acquisition and post-processing

Courtesy LIRMM, France – P. Maurine
Measurement of Susceptibility

Standards for susceptibility measurements, mostly up to 1GHz

<table>
<thead>
<tr>
<th>IEC 62132-2</th>
<th>IEC 62132-3</th>
<th>IEC 62132-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Bulk Current Inj. 1 GHz)</td>
<td>(Direct Power Int 1GHz)</td>
<td>(TEM/GTEM)</td>
</tr>
<tr>
<td>Most usual conducted method</td>
<td></td>
<td>Most usual radiated method</td>
</tr>
<tr>
<td>IEC 62132-8</td>
<td>IEC 62132-6 :</td>
<td>IEC 62132-9</td>
</tr>
<tr>
<td>(Ministrip 5 GHz)</td>
<td>(LIHA : 10 GHz)</td>
<td>(NFS 10 GHz)</td>
</tr>
</tbody>
</table>

Measurement of Susceptibility
Most usual conducted method
Most usual radiated method

Susceptibility characterization is much more complex and time consuming than emission: example of one DPI IO test

- Signal generator
- 10W Amplifier
- Printed Circuit Board
- Device under test
- Oscilloscope
- PC Monitoring
- IEEE Bus

Power increase loop until failure
Frequency loop 1 MHz – 3 GHz
Good signal
Failure signal
Zoom on Near-field Immunity

Near-field immunity coupling up to 6 GHz using a small loop (IEC 62132-9)

Magnetic loop

Result example

A. Boyer, Electronics Letters 2007

V. Models for EMC simulation
A Family of Models

Simulation Level

- Equipment
- Board
- Component
- Physical

Net
Dipoles
ICEM
LEECS
Spice

Complexity

- low
- medium
- high
- x-high

1 V(f), 1 Z(f)
10^1 dipoles
10^1 R, L, C, I
10^2 R, L, C, I
10^6 R, L, C, I

Global Modeling Approach

General flow to validate emission models for ICs

Simulations
- Core Model
- Package Model
- Probe Model
- Test board Model

Analog Time Domain Simulation
Fourier Transform

Measurements
- Frequency measurements
- Time-domain measure

Fourier Transform

Compare dBμV vs. frequency
Generic EMC model

The IC model usually includes two parts:

- **Passive Distribution Network (PDN)**
- **Internal Activity (IA)**
- **IOs (IBIS)**

**The die(s)**

- **Package leads (IBIS)**
- **Padframe**
- **On-package discrete components**

**Package**

IC

The IC model usually includes two parts:

- **Passive Distribution Network (PDN)**
- **Internal Activity (IA)**
- **IOs (IBIS)**

**The die(s)**

- **Package leads (IBIS)**
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**Package**

IC

IC Model for TEM Cell Simulation

**TEM cell model**

- **Capa coupling**
- **Inductor coupling**

**Limit of the package**

**Limit of the die**

To receiver

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A 32-bit Microcontroller Case Study

Infineon TriCore™ for automotive applications

R/n, L/n, C*n strategy for package model

On-chip decoupling

EMC of IC

Core current model

Core decoupling

Infineon TriCore™ measurement/simulation comparisons

- Correct envelop
- Reasonable match
- Simulation 15 dB above measurement starting 700 MHz
- Manual fit leads to 5 dB max difference

Radiated noise in GTEM cell (dBµV)

Frequency (MHz)

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Microcontroller susceptibility Model including injection path

- 16 bit micro-controller
- Direct power injection
- VDD Supply perturbation
- Sinusoidal mode
- Simulation criterion: VDD fluctuation over 20%

Power to induce failure in DPI (dBm)

Frequency (MHz)

VI. Design Rules for Improved EMC and Signal Integrity
Reduced the Inductance

Avoid power lines on long leads

Place VDD and VSS close to center

Place VDD-VSS close

- to reduce current loops that provoke magnetic field
- to increase decoupling capacitance that reduces fluctuations
Place Supplies Close to Strong Current Transients

Tools required to forecast strong di/dt effects
For 10 IOs, use one pair of Supply

9 I/O ports

Correct

Fail

Case Studies

Infineon Tricore

Virtex II
FPGA Comparison

Same power, same IO characteristics. The pin assignment and power supply strategy differ;

Xilinx Virtex-4 FF148
Altera Stratix II F1120

Returns spread evenly
Many regions bevoid of returns

Good design: moderate noise during IO switching

Poor design: x 5 mode switching noise

© Dr. Howard Johnson, "BGA Crosstalk", www.sigcon.com

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On-chip Decoupling

Why:
- to keep the current flow internal
- to reduce the supply voltage swing

Parasitic emission (dBµV) vs. frequency (MHz)

- No decoupling
- 1nF decoupling

Customer’s specification

Volt vs. time

On-chip Decoupling – Case study

- 1nF added close to the core
- More than 15 dB noise reduction
On-chip Decoupling

Filler-cap at the output buffer area

High speed port

Protection circuit

VDD

VSS

Core

On-chip Decoupling

Jitter on the Clock

© B. Vignon, Freescale SAS
Rule Reuse for Immunity

Decoupling capacitance is also good for immunity

Work done at Eseo France (Ali ALAELDINE)

VII. Future - What is next?

Susceptibility level

Normal Core

Isolated Core

RC Code

Frequency

Rule Reuse for Immunity

VII. Future - What is next?
Electromagnetic Reliability

Evolution of EMC characteristics over the lifetime

Infancy

30 years?
15 years?

EMR - Immunity

Low Temperature (-65°C) Accelerates Life Time – 15 years -> 408 H

10 dBm (factor 10)

Initial DPI meas.
After 15 years
And now: 10-100 GHz

Consumer electronics, telecoms to use this band soon (or now...)

(Parasitic Emission dBµV)

- Customer pressure
- Emission envelop
- Customer concern

Measure 10-100 GHz

- [s] Measurement is available (but costs a lot...)
- The GTEM concept could be extended to 100 GHz
- On-chip sampling
  Passive scanners

Freescale/Insa patent « Cube probe, in partnership with Univ. Carleton Canada
### Model Approaches

<table>
<thead>
<tr>
<th>Bandwidth (GHz)</th>
<th>Type</th>
<th>2005</th>
<th>2010</th>
<th>2015</th>
<th>2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 3 (IEC 62433)</td>
<td>Conduit</td>
<td>Ind. use (ICEM)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rayonné</td>
<td>Sol. exist</td>
<td>Ind. use</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(ICEM-radiated, dipole)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-18</td>
<td>Conduit</td>
<td>NOT known</td>
<td>Sol. exists</td>
<td>Ind. use</td>
<td></td>
</tr>
<tr>
<td>Rayonné</td>
<td>NOT known</td>
<td>Sol. exists</td>
<td>Ind. use</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18 – 40</td>
<td>Conduit</td>
<td>NOT known</td>
<td>NOT known</td>
<td>Sol. exists</td>
<td>Ind. use</td>
</tr>
<tr>
<td>Rayonné</td>
<td>NOT known</td>
<td>NOT known</td>
<td>Sol. exists</td>
<td>Ind. use</td>
<td></td>
</tr>
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</table>

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### … and Why Not?

- Imagine 0 dBμV designs
  - cancel all fields
  - 0 external di/dt
  - De-synchronized parts
- Imagine zero susceptibility designs
  - Clamp, filter
  - Protect, shield by design, materials
  - Defensive core
- RFI, ESD, EOS, EFT
- Critical supply
- Critical decision
- Reduce frequency
- Reduced VDD
- Smart capa management
- Redundancy
Who will contribute?

Industry

Academics

Recent publications in EMC of ICs

Conclusion
Conclusion

- Trend towards higher complexity and frequencies
- EMC investigated late in the design flow
- Mature standard measurement methods dedicated to ICs
- Golden rules for low EMC exist
- Soon, requirements up to 10 GHz
- In the future, 10-100 GHz EMC effects will be addressed
- A lot of room for invention, progresses in low emission and high immunity

References

Books

- www.springeronline.com

Tools

- www.ic-emc.org

Workshops

- www.emc-compo.org

Standards www.iec.ch

- IEC 61967, 2001, Integrated Circuits emissions
- IEC 62132, 2003, integrated circuits immunity
- IEC 62433, 2006, Integrated Circuit Model
Merci beaucoup(*)
The audience
Ross Carlton
The IEEE EMC society

(*) Thanks a lot