



93/146/CDV

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Also of interest to the following committees	Supersedes document		
Functions concerned			
<input type="checkbox"/> Safety	<input checked="" type="checkbox"/> EMC	<input type="checkbox"/> Environment	<input type="checkbox"/> Quality assurance

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Titre: CEI 62014.3: CEM des composants –
Partie 3 : Modèle électrique des circuits intégrés
(ICEM)

Title: IEC 62014-3: EMC for Component – Part 3:
Integrated circuits Electrical Model (ICEM).

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IEC 62014-3 Models of Integrated Circuits for EMI behavioral simulation

1 Scope

The objective of this **technical report (TR)** ICEM (Integrated Circuit Electrical Model) for Components is to propose electrical modeling for integrated circuit internal activities. This model will be used to evaluate electromagnetic behavior and performances of electronic equipment.

1.1 General

Integrated circuits integrate more and more gates on silicon and the technologies are faster and faster. To predict the electromagnetic behavior of equipment it is required to model IC interface switching and their internal activities as well. Indeed IBIS and IMIC models are focused mainly on interface activity predictions (cross talk, overshoot, ...).

This document describes a model for EMI simulation due to IC internal activities. This model gives more accurately the electromagnetic emissions of electronic equipment by taking into account the influence of internal activities. This model gives general data which could be implemented in different format such as IBIS, IMIC, SPICE, ...

During the design stage of the application that will exploit the IC, it becomes useful to predict and to prevent electromagnetic risks with CAD tool. Accurate IC modeling is necessary to run on these simulation tools.

Three coupling mechanisms of the internal activities for emission (Figure 1) are proposed in the ICEM model:

- Conducted emissions through supply lines,
- Conducted emissions through input/output lines,
- Direct Radiated emissions.

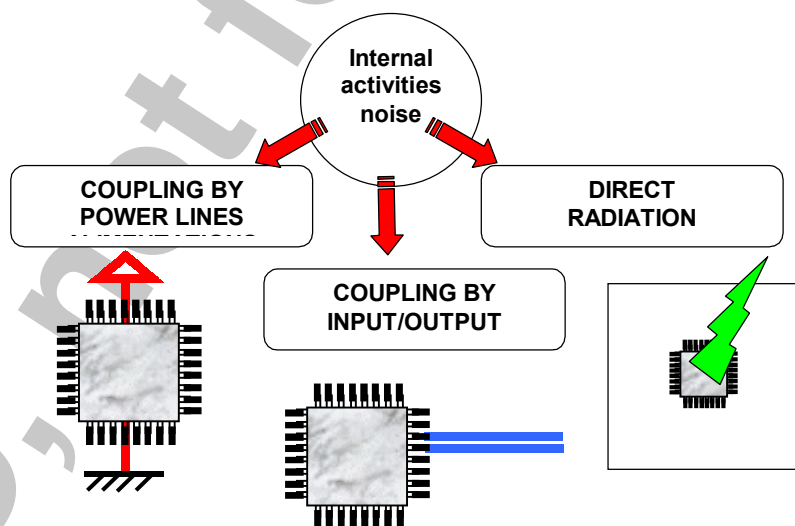


Figure 1 - Mechanisms for parasitic emission covered by ICEM

This document proposes a model that addresses those three types of coupling in a single approach. The elements of the model **would** be kept as simple as possible to ease the identification and simulation process.

1.2 Philosophy

The purpose of this document is to provide data to enable printed-circuit-board level (PCB) electromagnetic tools to compute the electromagnetic fields produced by integrated circuits and their associated PCB. These data can be extracted from measurement methods, as described in the IEC61967 standard, or obtained from IC simulation tools.

1.2.1 Origin of parasitic emission

The origin of parasitic emission in I.C is due to the current flowing through all the IC gates (I_{vdd} and I_{vss}) during high to low or low to high transitions as shown in figure 2.

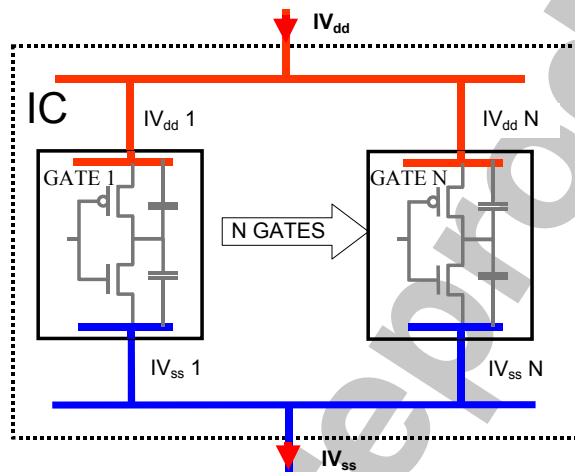


Figure 2 - The basic mechanism for parasitic emission is due to the current driving by all the gates

The combination of several hundred thousands of gates lead to very important peaks of current, mainly at rise and fall edges of the clock circuit. For example Figure 3 plots the number of gates switching versus the time for an I.C integrating 1 million transistors. Consequently, high current spikes are created inside the die and induce voltage drops of the internal voltage references.

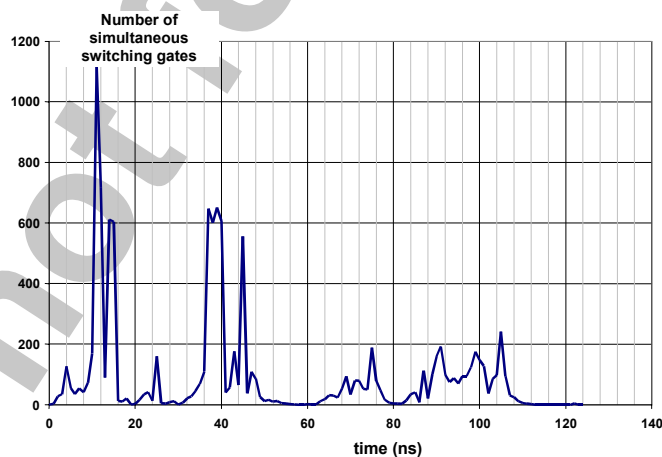


Figure 3 - Number of switching gates versus time

1.2.2 Conducted emission through power-supply lines

The current spikes created inside the die are partially reduced thanks to the on-chip decoupling capacitance. Anyhow, a significant portion of the current spikes is present at the power-supply pins of the chip. This current could be measured according to the IEC 61967 standard or other methods permitting to have the power-supply currents.

1.2.3 Conducted emissions through input/output lines (I/O)

The internal voltage drops generated by the current spikes create noise on the I/Os through direct connection, parasitic capacitive and inductive couplings and/or through common impedance. The PCB wires connected to the I/O can act as antennas and propagate electromagnetic emissions. The measurement set-up is done according to IEC 61967 standard.

1.2.4 Direct radiated emissions

The internal current flowing in low impedance loops generates electromagnetic fields which can be measured in near field according to the IEC 61967 standard.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All normative documents are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. Members of IEC and ISO maintain registers of valid International Standards.

IBIS - I/O Buffer Information Specification version 3.2

IEC 62014-1 : 93/91/CDV, Electronic behavioral specifications of digital integrated circuits I/O Buffer Information Specification (IBIS, Version 2.1)

IEC 93/67/NP : Models of integrated circuits for EMI behavioral simulation

IEC 62200 : 47A/575/NP, Integrated circuits, I/O Interface Model for Integrated Circuit (IMIC)

IEC 61967 part 1: Integrated Circuits, Measurement of electromagnetic emissions, 150KHz to 1GHz. General and definitions.

IEC 61967 part 2: Integrated Circuits, Measurement of radiated emissions, TEM cell method.

IEC 61967 part 4: Integrated Circuits, Measurement of conducted emissions, $1\Omega / 150\Omega$ method.

IEC 61967 part 6: Integrated Circuits, Measurement of RF current, Magnetic Probe Method.

3 Definitions

3.1 Electro Magnetic Compatibility EMC

Ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment.

3.2 Electro Magnetic Emission

Phenomenon by which electromagnetic energy emanates from a source.

3.3 Electro Magnetic Radiation

1. The phenomena by which energy in the form of electromagnetic waves propagates from a source into space.
2. Energy transferred through space in the form of electromagnetic waves.

4 ICEM models description

The proposed model includes 3 sections which describe the 3 coupling mechanisms of the internal activities for emission introduced in part 1:



- ICEM power-supply line model for conducted emissions through supply lines
- ICEM Input/Output for conducted emissions through input/output lines
- ICEM direct radiation for direct radiated emissions

Models are defined with electrical schematics described below for each IC pin.

4.1 ICEM power-supply line model

The I.C equivalent model shown in figure 4 is able to determine the peak harmonics spectrum and main resonances.

This model consists in:

- I_b : current generator,
- $L_{\text{pack}V_{\text{dd}}}$: package inductance of the positive supply V_{dd} ,
- $L_{\text{pack}V_{\text{ss}}}$: package inductance of the ground V_{ss} ,
- $R_{\text{pack}V_{\text{dd}}}$: package resistor of the positive supply V_{dd} ,
- $R_{\text{pack}V_{\text{ss}}}$: package resistor of the ground V_{ss} ,
- C_d : parasitic capacitor between V_{dd} and V_{ss} package pins,
- $R_{V_{\text{dd}}}$, series resistor of V_{dd} , bonding and die connection,
- $R_{V_{\text{ss}}}$, series resistor of V_{ss} , bonding and die connection,
- $L_{V_{\text{dd}}}$: inductance of V_{dd} , bonding and die connection,
- $L_{V_{\text{ss}}}$: inductance of V_{ss} , bonding and die connection.
- C_b : internal die capacitor.

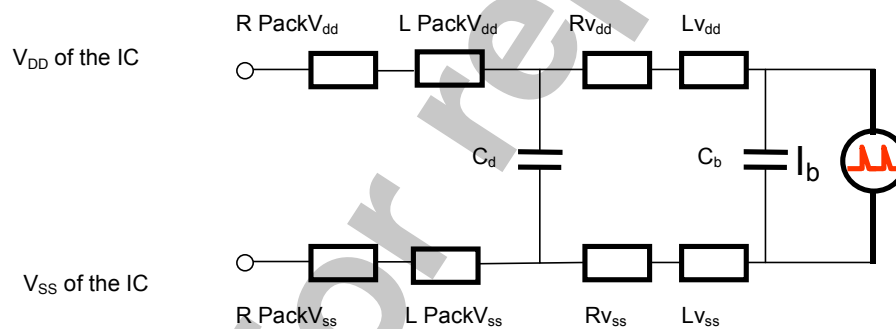


Figure 4 - Model of the IC supply lines

4.1.1 First and second order effects

The inductance of the package $L_{\text{pack}V_{\text{dd}}}$, $L_{\text{pack}V_{\text{ss}}}$, in series with the capacitance C_d create a first resonance, while the serial inductances $L_{V_{\text{dd}}}$, $L_{V_{\text{ss}}}$, in series with the local block capacitance C_b create a second resonance (Figure 5).

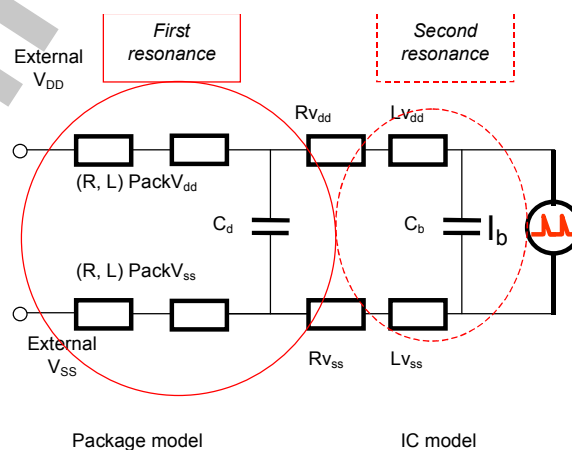


Figure 5 - Origin of primary and secondary resonance in the IC model

Taking into account second order effects in the proposed model give more accurate simulation results regarding measurement results, as shown in figure 6.

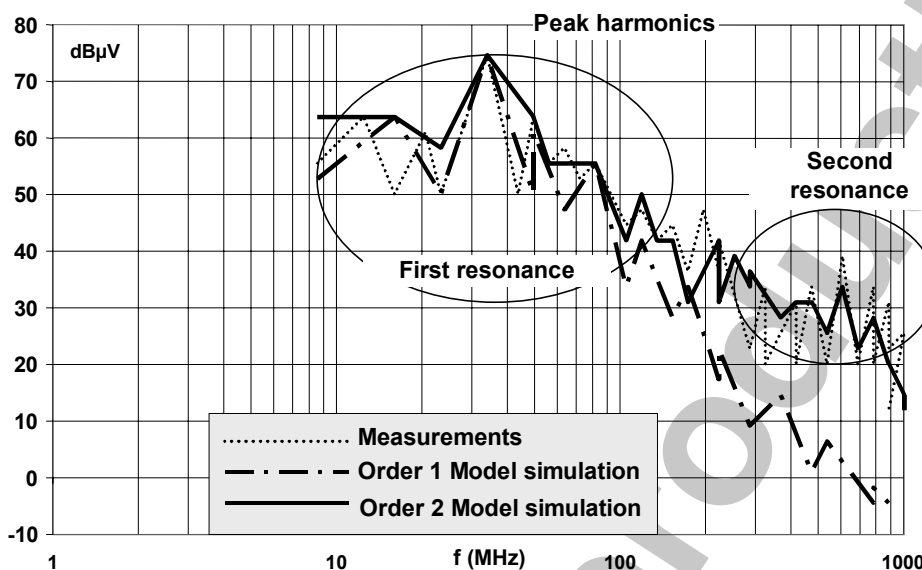


Figure 6 - Comparison between simulation and measurements (IEC 61967-4, 1Ω method)

4.2 ICEM Input/Output

4.2.1 Single supply structure

Disturbances on I/O are mainly due to the current flow in the supply and ground impedances added to I/O stage. The ICEM Input/Output is modeled by the superposition of that internal current noise with functional signals.

Functional signals are described with model as IBIS, IMIC or SPICE. The I/O on which the simulation is performed could be active or not. When other I/O's are activated on the same power lines a new equivalent current generator, $I_{i/o}$, representing peripheral activity, must be added in parallel to the generator representing the internal activity I_b .

The schematic of the model is reported in figure 7.

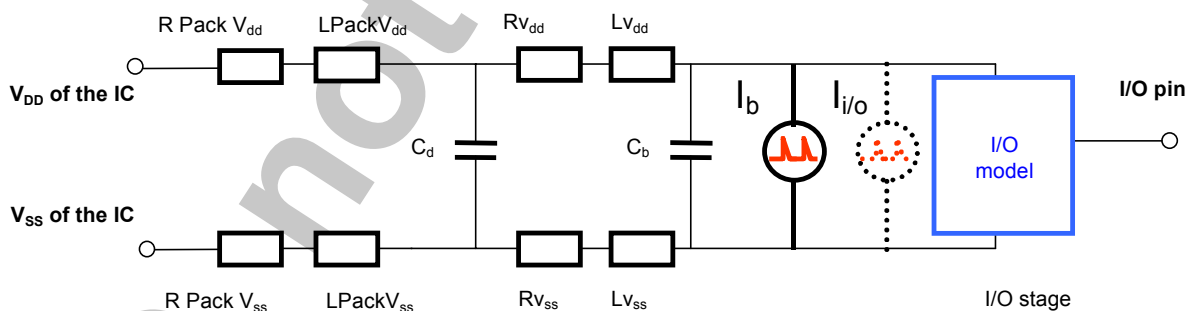


Figure 7 - Coupling between core and I/Os

Note: Frequency limits of functional I/O models would be take into account for EMC high frequency simulation. For instance a second order model would be defined, bonding and package elements, to simulate the resonances.



4.2.2 Multiple supplies structure

In many cases, the core supply and the I/O supply have separate internal networks. The core model is still identical, but two supplementary components are inserted, as illustrated in figure 8. The first parameter, named Z_{sub} , accounts for the substrate coupling path between the core V_{SS} and the I/O V_{SS} . The second parameter is the decoupling capacitance between I/O supplies, named C_{io} .

When other I/O's are activated on the same power lines a new equivalent current generator, $I_{i/o}$, representing peripheral activity, must be added to the generator representing the internal activity I_b .

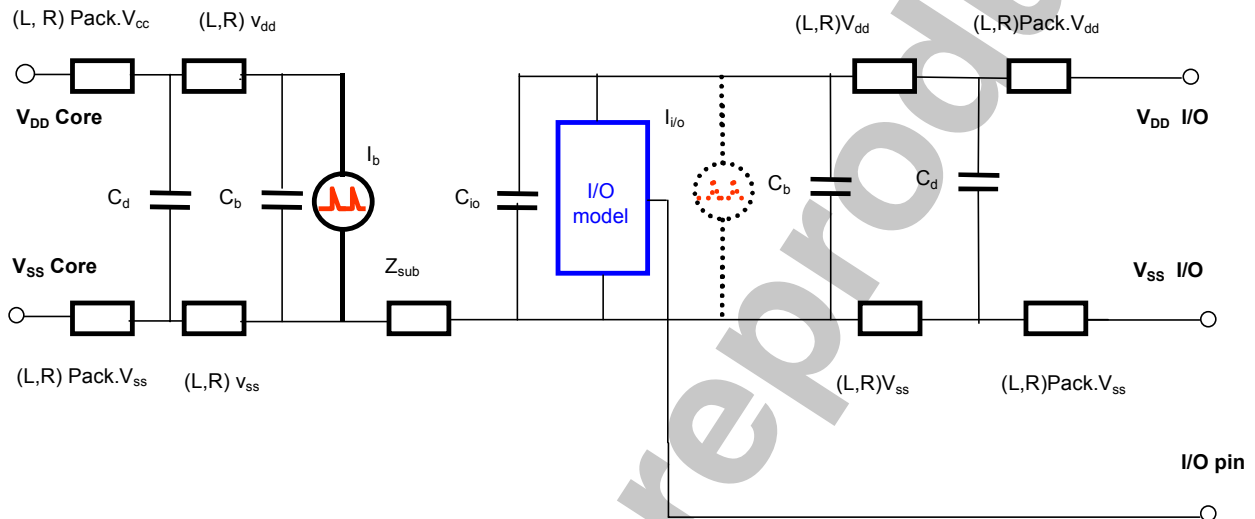


Figure 8 - Coupling between core and I/Os in the case of separate supplies

Note: Frequency limits of functional I/O models **would** be taken into account for EMC high frequency simulation. For instance a second order model **would** be defined, bonding and package elements, to simulate the resonances.

4.3 ICEM direct radiation

Electromagnetic emission could radiate directly from IC itself. The level is closely linked to current flowing in internal loops on package and on die.

The radiated electromagnetic emission **will** be characterised by measurement methods which measure direct radiation as for instance described in IEC 61967-2 in TEM cell.

Figure 9 shows measurement results in TEM cell with 2 microcontrollers

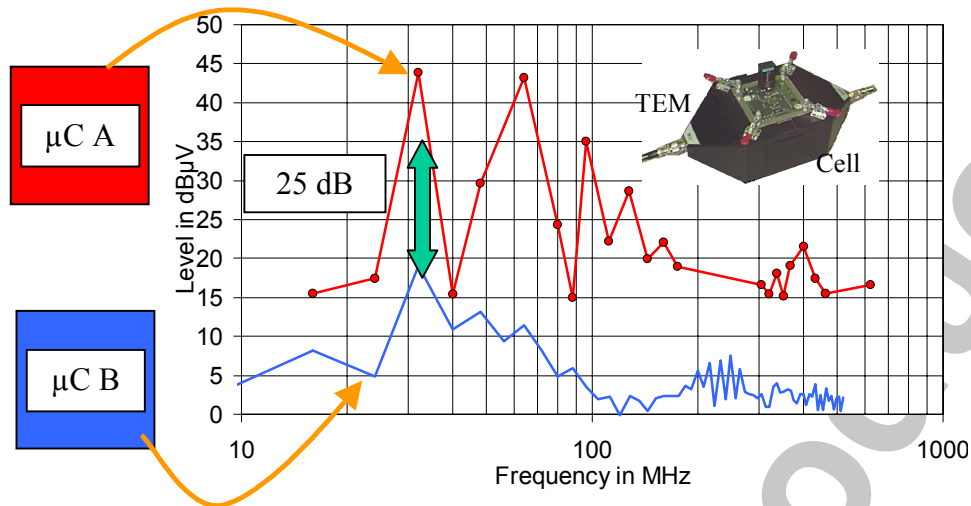


Figure 9 - IC direct emissions measured in TEM cell

Model parameters **would** be electrical parameters as internal currents and geometrical parameters as die size, internal loops area and package characteristics.

4.3.1 ICEM direct radiated model

This model **would** be based on an equivalent representation with dipoles.

It **will** be possible to implement it in models like IBIS, IMIC or SPICE.

The model is under definition and will be completed in future.

5 ICEM models parts details

The model parts are detailed in this section. We review the current generator I_b , the decoupling capacitance, the serial resistances and inductances and the local block capacitance.

Methods to determine model parts values are also considered in this section.

5.1 Passive parts parameters

Passive components of the model are: $L_{\text{pack}V_{\text{dd}}}$, $L_{\text{pack}V_{\text{ss}}}$, C_d , $R_{V_{\text{dd}}}$, $R_{V_{\text{ss}}}$, $L_{V_{\text{dd}}}$, $L_{V_{\text{ss}}}$, C_b , $C_{i/o}$, and Z_{sub} .

$L_{\text{pack}V_{\text{dd}}}$, $L_{\text{pack}V_{\text{ss}}}$ are package inductances.

C_d represents the parasitic capacitor between V_{dd} and V_{ss} package pins.

$R_{V_{\text{dd}}}$, $R_{V_{\text{ss}}}$ series resistances of the supply network modelizes the metal interconnect that connects the block supply to the main supply ring, which goes to the external supply through specific pads.

$L_{V_{\text{dd}}}$, $L_{V_{\text{ss}}}$ serie inductances of the supply network modelize the metal interconnect that connects the block supply to the main supply ring.

C_b is the internal die capacitor, placed in parallel with the local current generator. It accounts for the equivalent decoupling capacitance of the block.

$C_{i/o}$ is the internal die capacitor, placed in parallel with the I/O block (figure 8). It accounts for the equivalent decoupling capacitance between I/O's power supply lines.

Z_{sub} coupling impedance is valid for most CMOS technologies with P-type substrate. It accounts for the substrate coupling path between the core V_{ss} and the I/O V_{ss} .

Value ranges of these components are reported in table 1.

Table 1 - Value range of the model parameters

Part name	Min value	Max value
$L_{packV_{dd}}, L_{packV_{ss}}$	1nH	10nH
C_d	10pF	100nF
$R_{V_{dd}}, R_{V_{ss}}$	0,1 Ω	10 Ω
$L_{V_{dd}}, L_{V_{ss}}$	1nH	20nH
C_b	10pF	100nF
$C_{i/o}$	10pF	100nF
Z_{sub} dc value	0 Ω	100 Ω

These values are for informative purpose only. They may vary with new technologies.

In order to perform accurate simulations, the values of these parameters **would** be accurately determined for each specific case.

5.1.1 Measurement of part values

Input impedance **would** be measured according to time domain reflectometry method (TDR) or with a network analyser,...

From the measurement results and the already known data (eg package) it's possible to extract all the part values using mathematical procedures.

5.1.2 Prediction of part values

Part values could be determined with IC design tools which compute the RLC parameters from geometrical and electrical characteristic of IC.

5.2 The current sources I_b and $I_{i/o}$.

The main source of parasitic emission considered in the model is the current source I_b . The current shape may consist of the time-domain description of the current in PWL (Piece Wise Linear) format (Figure 10).

Typical values for I_b are several mA, up to 1A for the amplitude, 0.1 to 5ns for duration, and 500ps to 50ns for the period. These values are closely dependent on the software running.

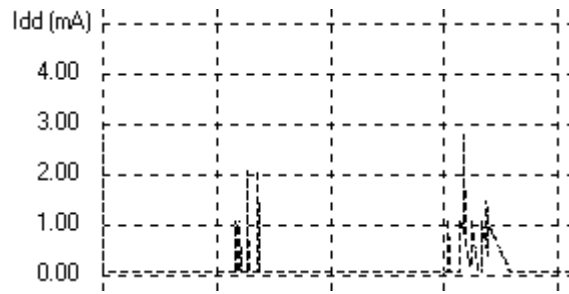


Figure 10 - Current source definition as a PWL description versus time

5.2.1 Measurement of I_b and $I_{i/o}$

External current **will** be measured, with or without I/O activities, but according to measurement method described in IEC 61967 standard. The software **would** be clearly described during that test.

A reverse engineering simulation of this external current with previous parameters permits then to extract the internal current value. In case of single supply line, the I_b current is obtained taking account of the $I_{i/o}$'s currents values following the interfaces are working or not. In case of multiple supply lines, each current is measured separately. So, the reverse engineering process is used similarly for the two currents.

Annex A

Simulation tools Implementation

The ICEM model described in this document includes additional elements specified to provide a capability to simulate EMC/EMI performances of a complete application or to optimize the PCB layout regarding EMC/EMI phenomena. Such simulation can also help to select active and passive components.

To perform an EMC/EMI simulation the different elements of the model previously defined need to be implemented in a software simulation tools.

This implementation and the exact definition of the final model depend on the software tool used and also base on the model type required, Spice for real time simulation or IBIS and IIMIC for behavioral modeling.

SPICE MODELING

If the software tools uses SPICE models, the element of the ICEM models have to be directly added to the spice electrical models so that the simulation can take into account the noise due to internal activity of the ICs.

IBIS MODELING

If the software tool require IBIS modeling format the element can be described as data files and these additional files need to added to the model description under IBIS format, for example specific keywords.

Evaluation a new IBIS release including EMC modeling is on going based on this document.

IMIC MODELING

Same comment as the ones done on IBIS modeling may be done on IMIC.

Evaluation to include the EMC elements of the ICEM model in the next release has to done.

**Annex B
(Informative)****REFERENCES****Part 1
EMC TASK FORCE CONTRIBUTORS**

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Part 2
MUNICH IBIS SUMMIT MEETING

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Integrated Circuits modeling

ICEM

**Integrated Circuits
Electromagnetic Model**

PROPOSAL : IEC 62014 - 3

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PLAN

- ICs AND EMC SIMULATION NEEDS
- UTE EMC TASK FORCE
- ICEM MODELS
 - Power lines contribution
 - I/Os contribution
- ICEM IMPLEMENTATION IN IBIS DATABASE
- CONCLUSION

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**ICs AND EMC
SIMULATION NEEDS**

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ICs AND EMC SIMULATION NEEDS

- **INTEGRATED CIRCUITS MANUFACTURERS.**
 - New ICs design have to take into account EMC/EMI
 - To include EMC in development phenomena need to be simulated.
- **PRINTED CARD BOARD DESIGN**
- **COMPLY EMC DIRECTIVES AND STANDARDS.**
 - Predict and improve EMC performances requires to be able to simulate phenomena
- **SIMULATION TOOLS** or behavioural model (like IBIS) available on the market for PCB simulation do not take into account EMC phenomena, mainly signal integrity.

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UTE EMC TASK FORCE

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	PERRAUD Richard	EADS CCR
	SAINTOT Pierre	ST MICRO ELECTRONIQUE
	SOUBEYRAN Amaury	EADS MSI
University	SICARD Etienne	INSA
	RAMDANI Mohamed	ESEO
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MODEL PROPOSAL IEC 62014 - 3

PROGRAM STATUS

- 1994 : WORKING GROUP UTE/CEF 93GT5 EMC
- 06 / 1997 : IEC 93 / 67 NP
- 1998 : DATE 98 / INTERNATIONAL TASK FORCE
- 2000 : DATE 2000 / IEC INTERNATIONAL EXPERTS MEETING
- 03 / 2001 : IEC 62014 - 3
CDV proposal sent to IEC for standard approval
- 03 / 2001 : DATE 2001 MUNICH IBIS SUMMIT MEETING



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MODEL PROPOSAL IEC 62014 - 3

ICEM MODEL

Integrated Circuits Electromagnetic Model

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MODEL PROPOSAL IEC 62014 - 3

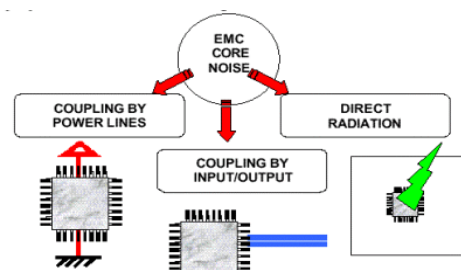
ELECTROMAGNETIC AND HF NOISE SOURCES

- **Power supply lines emission :**
Switching activity in different modules (Internal/peripheral)
High frequency current through package connections
- **I/O connections noise emission :**
Noise due to output fast signals and package characteristics
Noise coupling through package to the other I/O pins
Noise coupling through package to other powers supplies
- **IC Direct emission :**
Package Bonding and metal die connections

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MODEL PROPOSAL IEC 62014 - 3

ICEM model

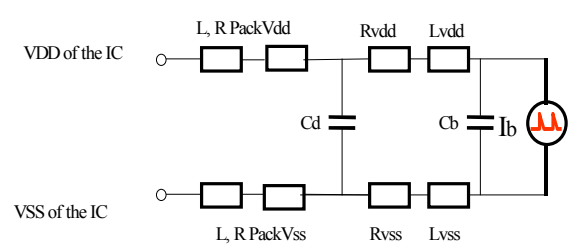


Mechanisms for parasitic emission covered by ICEM model

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MODEL PROPOSAL IEC 62014 - 3

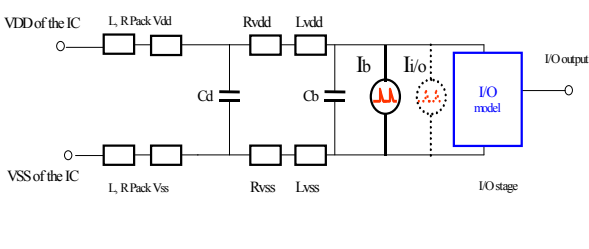
Power lines contribution



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I/Os contribution, single supply structure



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I/Os contribution, multiple supply structure

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ICEM IMPLEMENTATION IN IBIS DATABASE

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PACKAGE MODELING

Keyword [define package model]
 Keyword [manufacturer]
 Keyword [second order]
 Keyword [description]
 Keyword [number of pins]
 Keyword [pin numbers]

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PACKAGE L, R, C DESCRIPTION

Keyword [pin numbers]
 Keyword [All]
 Keyword [bonding]
 Keyword [package pin]

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Example of Package description from manufacturers

[Package]	Variable	Typ	Min	Max
R_pkg	0.1034	0.048	0.2592	
L_pkg	2.263e-09	1.098e-09	4.827e-09	
C_pkg	2.045e-13	8.363e-14	3.75e-13	

[Pin]	signal_name	R_pin	L_pin	C_pin	
1	PIN_1	NC	0.07963	1.849e-09	1.187e-13
2	PIN_2	NC	0.08791	2.116e-09	1.73e-13
3	PIN_3	NC	0.1445	3.071e-09	2.239e-13
4	PIN_4	NC	0.08285	1.841e-09	1.315e-13

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Example of Package description from manufacturers

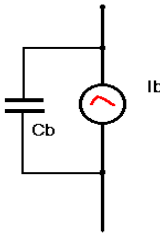
```

* CONDUCTOR LAYER NAME TYPE HEIGHT(MM) THICKNESS(MM) *
*****
* 11 LF 0.46000 0.01000
* 10 BW 0.47000 0.02540
*****
* MISC
Electrical Data By Pin (at DC):
Pin R (ohms) L (nH) C (pF)
Whole BW Whole BW Whole BW
1. 0.080 0.072 1.849 1.643 0.119 0.105
2. 0.088 0.065 2.116 1.489 0.173 0.108
3. 0.144 0.063 3.071 1.432 0.224 0.107
4. 0.083 0.061 1.841 1.390 0.132 0.106
5. 0.060 0.060 1.372 1.372 0.105 0.105
    
```

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CURRENT GENERATOR DESCRIPTION



[Ib generator]
[Cb capacitor]

Variable	Typ	Min	Max
C_pkg	2.045e-13	8.363e-14	3.75e-13

[Vdd Vss Pin]
[Ib current]

Variable	Typ	Min	Max
Ib (mA)	1	10	50
t (nS)	.5	1	1.5
	2	2.5	3
	3	3.5	4

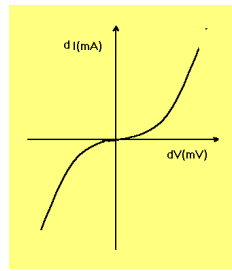
[Frequency]

Variable	Typ	Min	Max
F(MHz)	13	6	50

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INTER COUPLING POWER SUPLIES Zsub



[Zsub]
[Csub capacitor]

Variable	Typ	Min	Max
C_pkg	2.045e-13	8.363e-14	3.75e-13

[vss1 vss2 pins]
[z impedance]

Variable s	Typ	Min	Max
dI(mA)	.01	1	2
dV (nS)	.1	.2	.3
	.4	.5	.6
	.7		

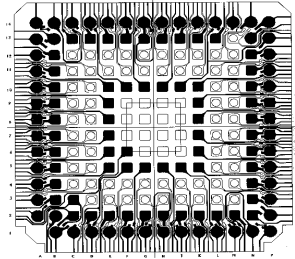
[Frequency]

Variable	Typ	Min	Max
F(MHz)	13	6	50

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DIRECT IC ELECTROMAGNETIC EMISSION



Emission Mainly due to package

Variables

- Pin length
- Frequency
- RLC (Resonances)

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CONCLUSION

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CONCLUSION

- ICeM Gives a capability to simulate EMC due to internal activity and of I/Os noise coupling
- ICeM model easy to add as modification od add on files to standards like IBIS
- ICeM model parameter can be obtained if data are not available from ICs manufacturers.

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CONCLUSION

ACTIONS PLAN TO PERFORM

- COOK BOOK to be written to explain how to obtain ICeM Model parameters. (First draft is on going)
- Evaluation through IBIS forum
- Integration in standard models database (For ex IBIS)
- PCB simulation tools integration to provide EMC simulation capability.
- Softwares Validation

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ANNEXE

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STUDY REASON

Mise en évidence de l'importance de l'activité interne sur le rayonnement du composant.

Niveau en dBµV **Mesures en TEM**

µC-A (fondeur A)
H ext. : 8 MHz
H cœur : 16 MHz

µC-B (fondeur B)
H ext. : 16 MHz
H cœur : 8 MHz

Même fonction interne
Activité externe
Commutation de 6 sorties
à 2 MHz sur 50pF

Les modèles actuels entraîne une erreur de simulation de 15 dB dans ce cas.

Il faut modéliser l'activité interne pour simuler le rayonnement

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