[reference]

Proposer France	Date of proposal October 2001
TC/SC UTE 47A EMC Task Force	Secretariat
Date of circulation	Closing date for voting

A proposal for a new work item within the scope of an existing technical committee or subcommittee shall be submitted to the Central Office. The proposal will be circulated to the P-members of the technical committee or subcommittee for voting, and to the O-members for information. The proposer may be a National Committee of the IEC, the secretariat itself, another technical committee or subcommittee, an organization in liaison, the Committee of Action or one of the advisory committees, or the General Secretary. Guidelines for proposing and justifying a new work item are given in ISO/IEC Directives, Part 1, Annex Q (see extract overleaf).

The proposal (to be completed by the proposer)

Title of proposal

Cookbook for Integrated Circuit model ICEM , project number 62014-3

Scope (as defined in ISO/IEC Directives, Part 3, 6.2.1)

This document specifies and describes parameters of models ICEM . That model proposal is for use with electromagnetic field calculation simulation tools.

☐ Safety	☒ EMC	☐ Environment	☐ Quality assurance

Purpose and justification (attach a separate page as annex, if necessary)

Target date (indicate the date by which the availability of the International Standard is considered to be necessary)

Relevant documents to be considered

Relationship of project to activities of other international bodies

DRAFT That document is a working preliminary document under construction

Integrated Circuit Electromagnetic Model (ICEM)

IEC 62014-3

Cookbook

Release 1.f
May 31, 2002

Authors:french committee UTE 47A EMC Task Force www.ute-fr.com

TABLE OF CONTENTS

1 INTRODUCTION

The objective of this cookbook is to describe parameters of standard ICEM (Integrated Circuit Electromagnetic compatibility Model) proposed as IEC 62014-3 [1] for modeling the radiated and conducted parasitic emission of integrated circuits on printed circuit boards. In addition this cookbook also proposes methods to determine ICEM parameters used by simulation tools.

1.1 General and philosophy

Today with increasing of IC performances, clock systems and faster transition time, IC are more and more at the origin of the electromagnetic behavior of the electronic equipment and systems. As a consequence, the level of parasitic emission increase with the technology scale down, as illustrated in figure 1-1.

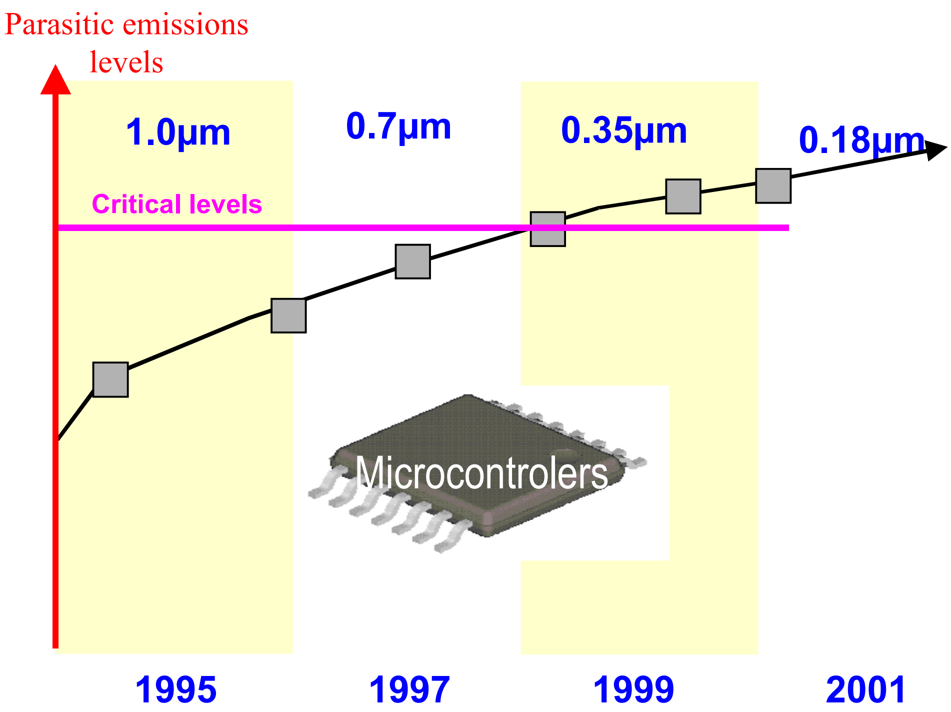


Figure 1-1: Increased maximum parasitic emission with the technology scale down (conducted emission)

During the design stage of the application that will exploit the IC, it becomes useful to predict and to prevent electromagnetic risks with EDA tool. Accurate IC modeling is necessary to run on these simulation tools [2].

Radiated noises in electronics systems are linked to IC EMC behaviour as well. Inside IC noise root causes are due to core activity and I/O interface switching . IBIS standard [3],[4] proposes models for interface stages , ICEM standard proposal introduces models for core activities . ICEM models will provide parameters for radiated and conducted emissioins simulation.

The purpose of the ICEM standard is to provide data to enable printed-circuit-board level (PCB) electro-magnetic tools to compute the electromagnetic fields produced by integrated circuits and their associated PCB.

Three emission mechanisms addressed are:

- Conducted emission through supply pins
- Conducted emission through input/output activities
- Radiated emission

1.2 Origin of parasitic emission

The origin of parasitic emission in integrated circuit is mainly the current flowing in each elementary gate, when its output is activated, either rising from logic level 0 to 1 (left figure 1.2) or from 1 to 0 (right figure 1.2).

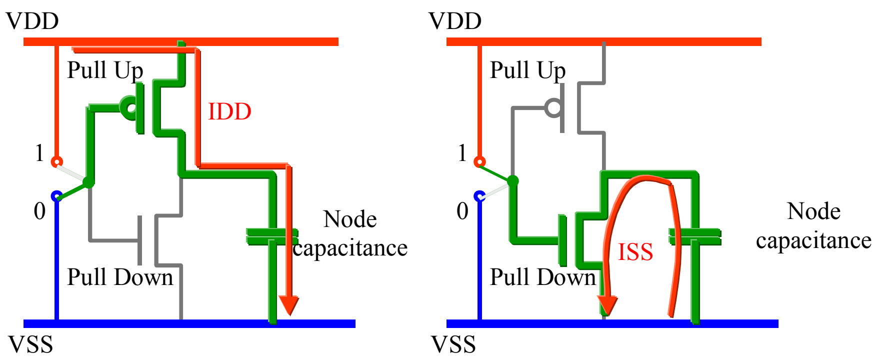


Figure 1.2: basic mechanism for parasitic emission during gate switching

The combination of several 100 thousands of gates lead to very important peaks of current, mainly at rise and fall edges of the circuit clock. Figure 1.3 reports the switching activity over one cycle of 140ns of a 16 bit micro-controller, including approximately 1Million transistors. The simultaneous switching hits 1200 gates at time 60ns. Consequently, very severe current spikes are created inside the die and induce a fluctuation of the internal voltage reference (ground-bounce of the VSS supply, bounce of the VDD supply).

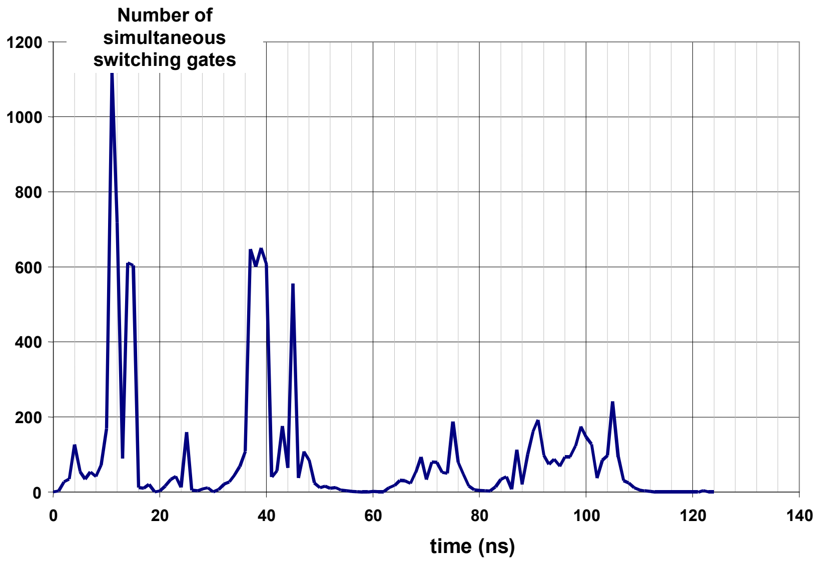
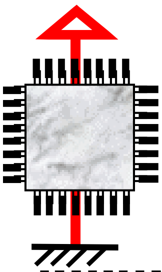
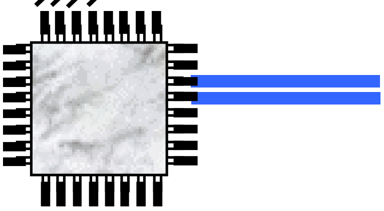


Figure 1.3: Simultaneous gate switching creates severe current peaks at clock edges

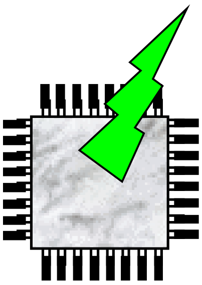
Three mechanisms for emission are discussed:



- *Conducted emission through supply lines*. Conducted emissions are due to the switching activity of core and buffers which induces current drops on the supply pins of the chip.



- *Coupling by I/Os.* The current spikes provoked by the internal core may be measured on the I/Os of the circuit, although not activated. The PCB wires connected to the I/O serve as antennas for the energy



- *Radiated coupling*. The internal current flow and resulting ground-bounce inside the chip are responsible of a radiated emission.

ICEM proposes a model that addresses the three types of coupling in a unique approach. The components are kept as simple as possible to ease the identification and simulation process.

2 Model structure

Models structure are detailled in the document IEC 62014-3, Integrated Circuit Electromagnetic Model (ICEM).Models proposed in that standard are general and generic, they describe EMC behavior, as IBIS for electrical behavior, rather than detailled physical structure described with SPICE-like simulator.

4 examples of model are proposed in that standard, 1 for supply lines, 2 for I/O lines regarding the supply structure and 1 for radiated effects from IC itself.

2.1 Power supply lines model

Model structure is proposed in figure 2.1.

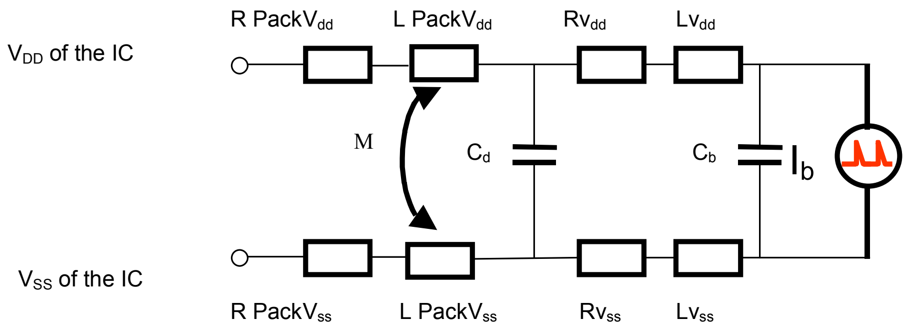


Figure 2.1: Model of the IC supply lines

Parameters of that model are defined as following:

- I_b : current generator,
- $LpackV_{dd}$: package inductance of the positive supply V_{dd},
- $LpackV_{ss}$: package inductance of the ground V_{ss},
- M : mutual package inductance ,
- $RpackV_{dd}$: package resistor of the positive supply V_{dd},
- $RpackV_{ss}$: package resistor of the ground V_{ss},
- C_d : parasitic capacitor between V_{dd} and V_{ss} package pins,
- Rv_{dd} : series resistor of V_{dd}, bonding and die connection,
- Rv_{ss} : series resistor of V_{ss} , bonding and die connection,
- Lv_{dd} : inductance of V_{dd}, bonding and die connection,
- Lv_{ss} : inductance of V_{ss}, bonding and die connection,
- C_b : internal die capacitor.

2.2 I/O lines model

Regarding the stucture of the power supply , 2 models are defined.

2.2.1 Single supply structure

With I/Os, the core coupling to the I/O is done by connecting the I/O structure, as defined in IBIS model to the internal supply of the chip. The schematic diagram of the model is reported in figure 2.2.

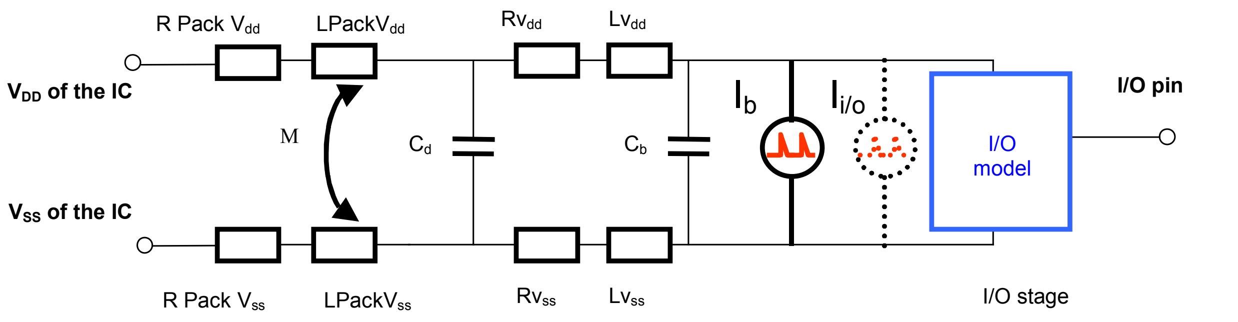


Figure 2.2: I/O lines model

Comparated to the supply line models, 2 parameters are added on that models:

- Ii/o : current generator for other I/O's activity
- I/O model : IBIS modelling

2.2.2 Multiple supply structure

In many cases, the core supply and the I/O supply have separate internal networks. The schematic diagram of the model is reported in figure 2.3.

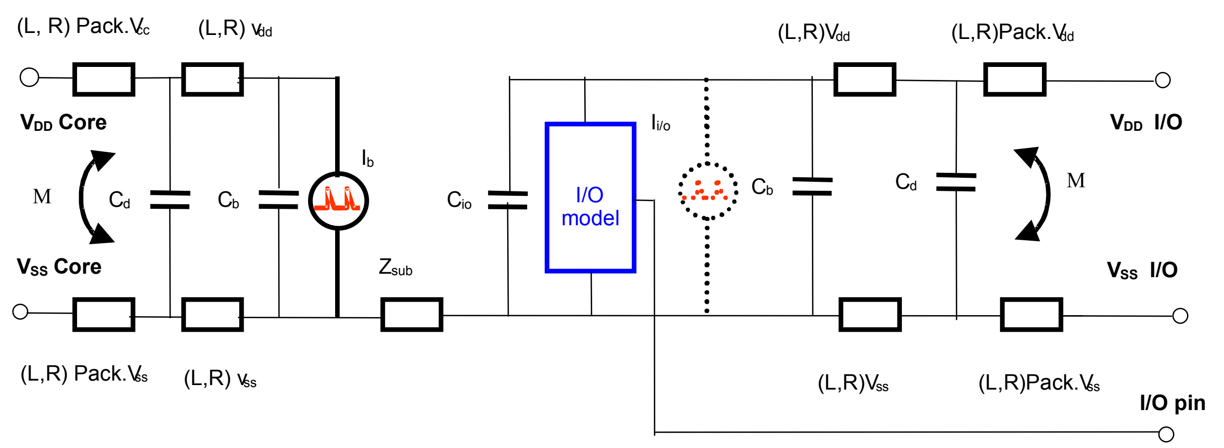


Figure 2.3: I/O line model

The core model is kept identical, but 2 additional components are inserted.

- Zsub: substrate coupling path between the core Vss and the I/O Vss. This coupling is valid for most CMOS technologies with P-type substrate. The typical value of Zsub is several ohms.
- Cio : decoupling capacitance between I/O supplies

2.3 Radiated model

This model would be based on an equivalent representation with dipoles.

The model is under definition and will be completed in future

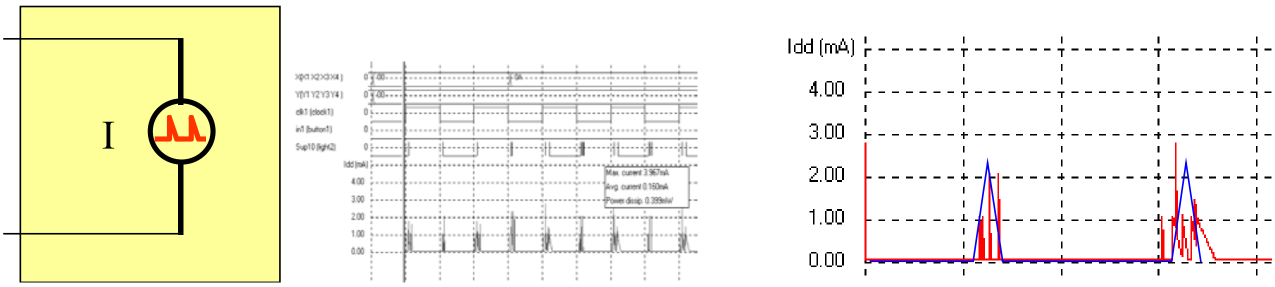
3 Model parameters extraction

For each models, 3 main generic kind of parameters can be separated, current generator, passive elements and direct radiation dipole.
This chapter describes how to get each group of parameter either with default value, or with measurement methods or with a predictive approach.

3.1 Current generators extraction

This section describes determination of models parts Ib or I i/o.

The current shape may consist either of the time-domain description of the current (Figure 3.1-a, 3.1b) or as an equivalent triangular waveform (figure 3.1-c).



(a) current generator (b) time-domain aspect of I (c) equivalent triangular model

Figure 3.1: Current source definition either as a detailed description versus time or by an equivalent triangular model

3.1.1 Default values

Typical values for Ib are several mA, up to 1A for the amplitude, 0.5 to 5ns for duration, and 500ps to 50ns for the period. Table 1 and 2 permit to obtain default values of Ib and Ii/o for main CMOS technology. To calculate total current it should be considered that from 1 to 10 percent of cells are switching simultaneously.

Technology CMOS	Year	Supply (V)	Cell Density (/ mm^2)	Clock frequency (MHz)	Peak gate current (mA/gate)
1.2µm	1985	5V	1500	4-50	1.1
0.8µm	1990	5V	4000	4-90	0.9
0.5µm	1993	5V	7000	8-120	0.75
0.35µm	1995	5-3.3V	13000	16-300	0.6
0.25µm	1997	5-2.5V	18000	40-450	0.4
0.18µm	1999	3.3-2.0V	22000	100-900	0.3
0.12µm	2001	2.5-1.2V	28500	150-1200	0.2

Table 1: Typical logic gate current and driver current for various technologies

Example to calculate I:

Cell density ASIC in 0.5µm is around 7000. The probable number of cells switching of 3x3mm² is approximately 7,000 x 9 = 63 kgates.Considering that in average 10% of cells are switching simultaneously, the probable CPU current at each clock edge is 63kgates x 10% x 0.75mA= 4725mA.

CPU technology	Total number of logic cells	Synchronous switching on clock edge
8 bits CISC	3000-5000	300-500
8 bits RISC	3000-5000	300-500
16 bits CISC	15,000-20,000	1500-2000
16 bits RISC	12,000-18,000	1200-1800
32 bits CISC	40,000-60,000	4000-6000
32 bits RISC	40,000-60,000	4000-6000

Table 2: Typical number of logic gates vs. Core complexity

Example:
a 16 bit RISC micro-controller fabricated in 0.25µm technology has approximately 15,000 gates. The probable CPU current at each clock edge is $15e^3$ x 10% x 0.4mA= 600mA.

3.1.2 Measurement Method

The measurement of the current I flowing trough the IC supply pin can be performed using the methods described in the IEC standard 61967 part4 (1Ω /150Ω method) [5] or with different probes as a current or a differential probes, not today an IEC standards.

The 1Ω /150Ω method measure the current in serial 1Ω in ground. Current probe method measure the current in the Vdd line. Figure 3.2 describe these 2 methods.

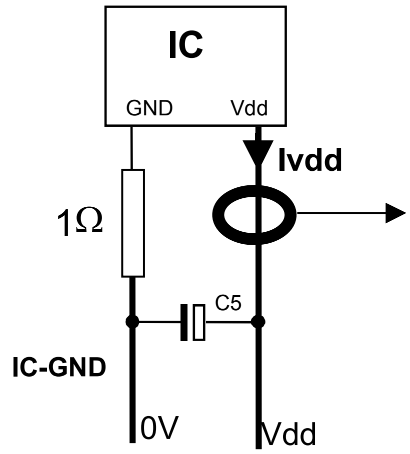


Figure 3.2: Current measurement

External current will be measured, with or without I/O. A reverse engineering simulation of this external current with previous parameters permits then to extract the internal current value. In case of single supply line, the I_b current is obtained taking account of the $I_{i/o}$'s currents values following the interfaces are working or not. In case of multiple supply lines, each current is measured separately. So, the reverse engineering process is used similarly for the two currents.

3.1.3 Prediction

Simulation design tools used by IC manufacturer can be used to evaluate that current.

3.2 Passive elements extraction

This section describes extraction of model parts R ,L, M, C :

- LpackV_{dd} : package inductance of the positive supply V_{dd},
- LpackV_{ss} : package inductance of the ground V_{ss},
- M : mutual package inductance,
- RpackV_{dd} : package resistor of the positive supply V_{dd},

- $RpackV_{ss}$: package resistor of the ground V_{ss},
- C_d : parasitic capacitor between V_{dd} and V_{ss} package pins,
- Rv_{dd} : series resistor of V_{dd}, bonding and die connection,
- Rv_{ss} : series resistor of V_{ss} , bonding and die connection,
- Lv_{dd} : inductance of V_{dd}, bonding and die connection,
- Lv_{ss} : inductance of V_{ss}, bonding and die connection,
- $C_{b,}$: internal die capacitor.

3.2.1 Default values

Values for passive elements could be deducted from typical values.

3.2.1.1 Series impedances and mutual

The series resistance and inductance of the supply network model the metal interconnect that connects the block supply to the main supply ring and bonding.

Part name	Min value	Max value
$LpackV_{dd}$, $LpackV_{ss}$	1nH	10nH
M	0	10nH
Rv_{dd}, RV_{ss}	0,1Ω	10Ω
LV_{dd}, LV_{ss}	1nH	20nH
Z_{sub} dc value	0Ω	100Ω

In the case of on-chip voltage regulator, the parameter Rvdd may account for the equivalent resistance of the device connected between the external and internal supply, as illustrated in figure 3.4.

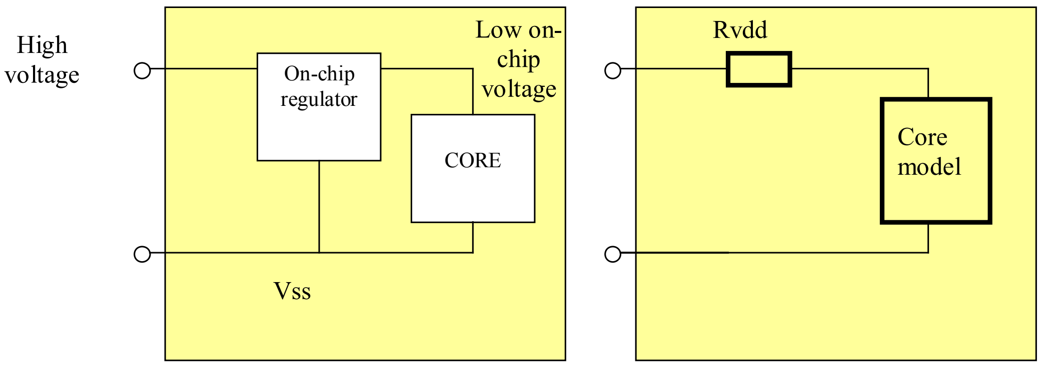


Figure 3.4: Series resistance as an equivalent model for the on-chip voltage regulator.

In that case, typical value for Rvdd may range from 10 to 500 Ohm.

3.2.1.2 Parasitic capacitor

The parasitic capacitance on the package is called Cd. It represents the total capacitance between the power supply package structure, as illustrated in figure 3.3.

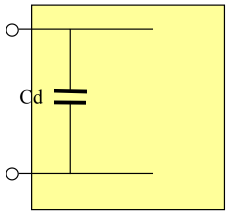


Figure 3.3: parasitic capacitance

Part name	Min value	Max value
C_d	10pF	100nF

3.2.1.3 Internal die capacitance

The internal die capacitance on the chip is called Cb. It represents the total capacitance between the power supply rails on chip. In most cases, this capacitance is a physical coupling between the internal supply rails VDD (positive supply) and the ground rail VSS (0V supply). The origin of the capacitance Cd is rail to rail capacitance, junction capacitance and interconnect capacitance.

This capacitance is placed in parallel with the local current generator Ib. It accounts for the equivalent decoupling capacitance of the block. Separating internal die capacitance from the parasitic capacitance Cd creates a second LC network (Lvdd, Cb, Lvss) at the origin of a secondary resonance (Figure 3.6).

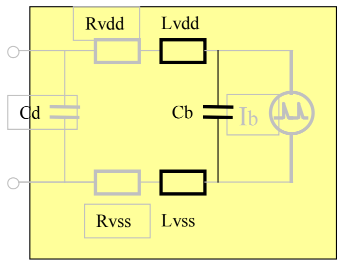


Figure 3.6: internal die capacitance

Technology CMOS	Year	Supply (V)	Cell Density (/mm^2)	Capa (fF/gate)	Decoupl Capa (fF/gate)
1.2µm	1985	5V	1500	60	10
0.8µm	1990	5V	4000	40	8
0.5µm	1993	5V	7000	30	7
0.35µm	1995	5-3.3V	13000	25	6
0.25µm	1997	5-2.5V	18000	20	5
0.18µm	1999	3.3-2.0V	22000	15	6
0.12µm	2001	2.5-1.2V	28500	10	8

Table 3: Typical internal die capacitance per gate and per interconnect for various technologies

Example:
Cell density is around 18,000 in 0.25µm technology internal die capacitance of 3x3mm2 ASIC in 0.25µm is 162e^3 x 5fF =810pF

3.2.2 Measurement method

RLC model value of IC are measured by network analyzer (N.A) and a specific PCB test board. A power-supply is connected to the network analyzer in order to supply the IC under test. A SMA connector should be used to connect directly the power pin of the IC under test in order to minimize parasitic effects of the connection. The ground pin is soldered directly on the ground layer of the PCB.

The figure 3.7 shows the setup used to extract the RLC model value of the I.C.

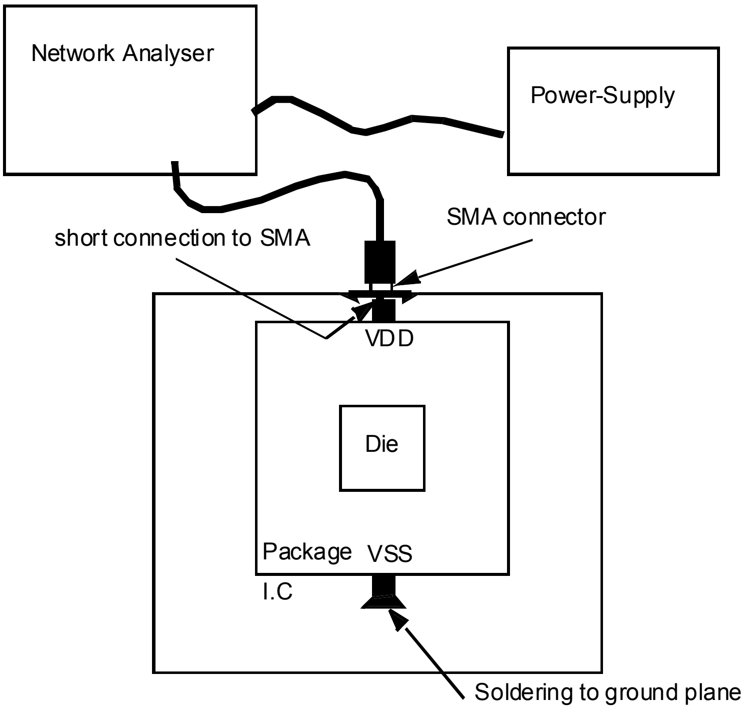


Figure 3.7 . Test setup to measure the RLC model of the package and die.

The impedance model is extracted from the measurement, as shown in the figure. 3.8. This plot shows the impedance versus frequency in dB-log scale, which can generally, be represented by a RLC model. That example presents a first order resonance,due to negligible Cd effects.
At the frequency resonance this impedance is purely resistive and gives the global resistance (RpackVxx+RVxx) of both package and internal power rails.
Below the resonance frequency the impedance is capacitive and due to the internal die capacitance Cb .The impedance falls off with frequency at a rate of 20dB per decade. The internal die capacitance can be calculated with the formula included in the figure 3.8 at a frequency which can be chosen at a decade below the resonance frequency.
Above the resonance, the impedance is inductive and due to the global inductance (LpackVxx+LVxx). This impedance increases with the frequency at rate of +20dB per decade.

By choosing a frequency which is a decade above the resonance frequency, this inductance can be calculated by using the formula included in the figure 3.8. The magnitude of the impedance Z in dBΩ is referenced to 50Ω .

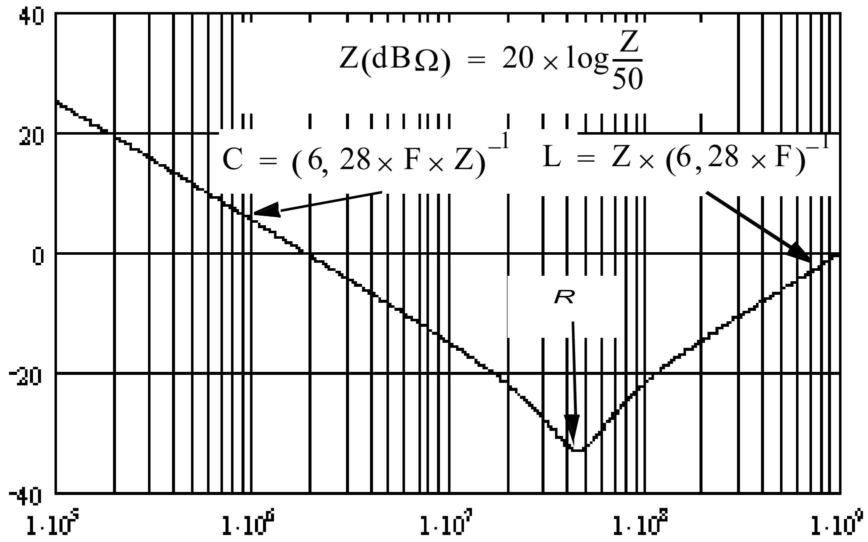


Figure 3.8 . Plot of the package and die impedance versus frequency.

Equivalent RLC model is measured on I.C. The VDD and VSS impedance models are assumed to be symetrical therefore inductance and resistance values could be divided by two.

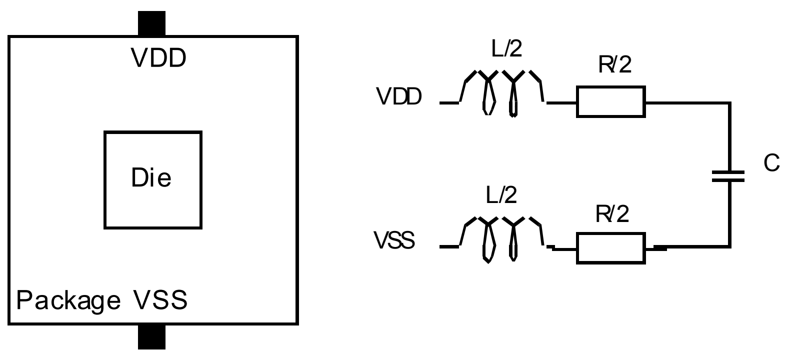


Figure 3.5. Equivalent RLC model of the I.C.

3.2.3 Prediction

EDA tools used by IC manufacturer may be used to evaluate all passive parameters .

3.3 Direct radiation parameter extraction

This model would be based on an equivalent representation with dipoles.The model is under definition and parameters extraction methods will be described in future.

References

[1] IEC 62014-3 : Models of integrated circuits for EMI behavioral simulation, ICEM

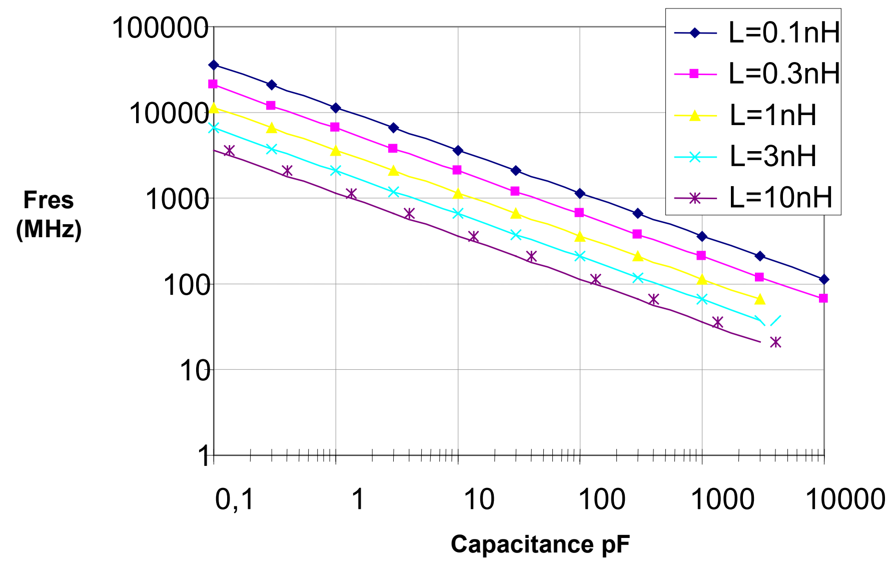
[2] IEC 93/67/NP : Models of integrated circuits for EMI behavioral simulation

[3] IBIS -I/O Buffer Information Specification version 3.2

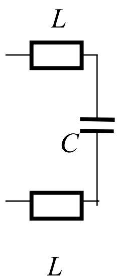
[4] IEC 62014-1 : 93/91/CDV, Electronic behavioral specifications of digital integrated circuits I/O Buffer Information Specification (IBIS, Version 3.2).

[5] IEC 61967 part4 : Integrated Circuits, Measurement ofElectromagnetic Emissions, 150 KHz to 1GHz : 1Ω/150 Ω Methods

Annex A : primary resonance table



Helps to forecast the resonance frequency from L & C



LC resonance frequency formulation for varying L and C

$$fres = \frac{1}{2\pi\sqrt{2.L.C}}$$