

# On the Prediction of Near-field Microcontroller Emission

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**Abstract**— This paper details a predictive approach for the evaluation of the magnetic field radiated by microcontrollers. The simulation is based on the radiation of elementary current dipoles corresponding to the current flowing in supply inductances. A CMOS test chip including six microcontroller cores has been scanned for validation purpose. Preliminary comparison show interesting similarities between measured and simulated scan, which build a valuable link between electrical macro-models and near-field electromagnetic formulations.

**Keywords:** IC, parasitic emission, near-field scanning, dipole

## I. INTRODUCTION

There is a growing demand for simulation of parasitic emission of electronic systems at early stages of the design, for which the integrated circuit noise plays a key role. The new step forward in microelectronics integration is the *system-in-package* approach where integrated circuits are stacked or placed very close to each other, which rises important issues to ensure the electromagnetic compatibility of such systems.

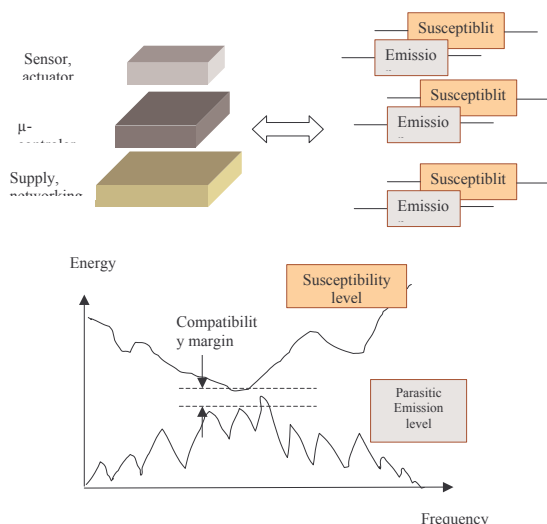


Figure 1. System-in-package are a stack of several integrated circuits, each of them having parasitic emission and susceptibility thresholds that should leave a sufficient safety margin

Accurate simulations of integrated circuit emission have been demonstrated by several authors, for both conducted emission using the 1-Ohm serial resistance standard and the radiated emission in TEM Cell [1].

An important effort has been dedicated the past recent years on standard modeling approaches for predicting the integrated circuit emission [2]. In parallel, near field scanning has been widely used to exhibit “hot spots” at the surface of integrated circuits and to guide IC designers for reducing the parasitic emission [3].

However, the link between electrical macro-models such as described in [2] and the near-field scanned information has not extensively studied. Our goal is to investigate the possible reuse of these simple electrical models and dipole-based magnetic field predictions. The first part of the proposal describes the test chip used for this study, the second part focuses on the simulation approach itself, and the last part compares simulations and measurements.

## II. CESAME TEST CHIP

The CESAME test chip is dedicated to the characterization of conducted and radiated emissions from six identical logic cores, each having a specific design technique which aims to reduce parasitic emissions. The main goal of the test chip was to validate these design rules and to quantify the benefits in terms of reduced parasitic interference. The most interesting results have been presented in [4].

The internal structure of CESAME is outlined in Fig. 2. Six logic core blocks are implemented in the same die. All these blocks have an identical structure based on latches, a clock tree and standard gate which reflect a standard core activity. Among these cores, two structures are worth of interest in our study: the normal core called “NORM” which is supposed to be noisy, and the “RC” core with includes a series resistor on the supply tracks and a local on-chip decoupling to feature low parasitic emission.

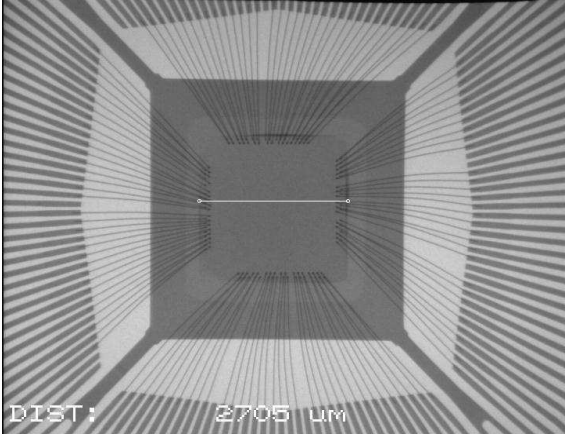
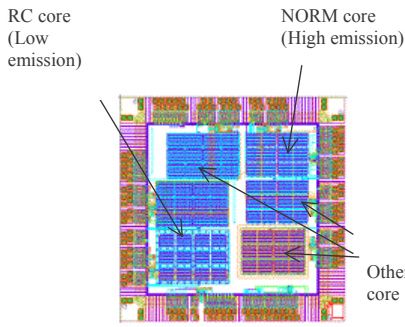


Figure 2. CESAME structure and partial view of the TQFP 144 pin package

The CESAME circuit includes 0.7 Million devices on a 2.7 mm x 2.7 mm die. The test chip is mounted on a TQFP144 package (20x20mm) and associated with a dedicated test board, which has been designed to explore the radiated, conducted and on-chip measurements according to existing standards [1]. From early studies [4], it has been shown that the gain in terms of conducted and radiated noise is around 15dB between the two cores, thanks to the serial resistance combined with an on-chip decoupling capacitance close to the current noise source (Figure 3).

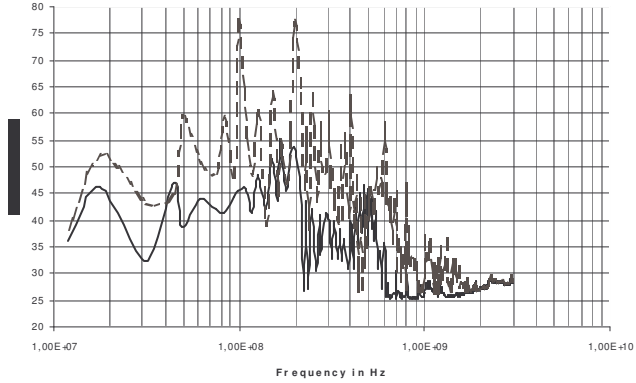


Figure 3. Measured conducted emission showing a significant reduction of the noise in the RC core as compared to the NORM core

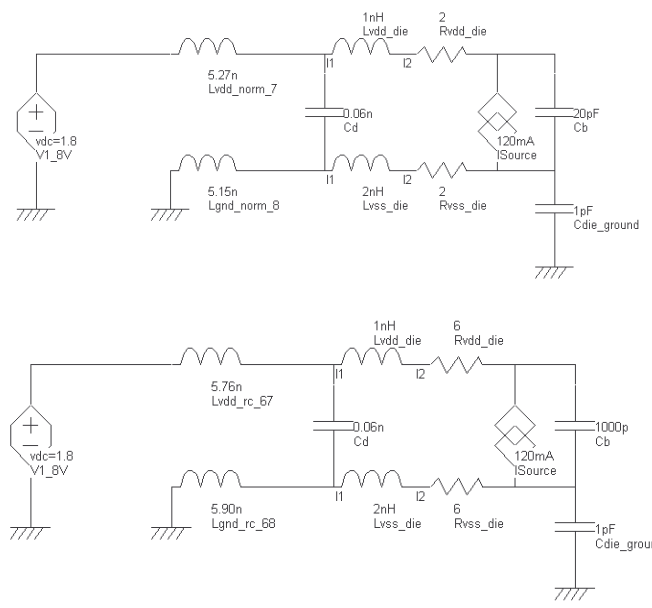


Figure 4. Schematic diagram of the NORM Core (upper figure) and RC Core (lower figure)

An electrical model has been setup and may well predict the emission of the two different cores. The schematic diagram of the CESAME cores are shown in figure 4. As can be seen on the right part, the current sources *ISource* are identical for NORM and RC core. The main difference concerns the serial resistance (*Rdd\_die*, *Rvss-die*) and the local decoupling capacitance *Cb*. The access inductance of the package is almost the same for RC and NORM cores. Good correlations between measured and simulated spectrum according to IEC 61967 standard [1] have been demonstrated. From these bases, our next goal is to extrapolate the near-field magnetic field.

### III. GENERAL APPROACH FOR COMPARING MEASUREMENTS AND SIMULATIONS

The general flow used to achieve a comparison between near-field measurement and simulated magnetic field emission is proposed in figure 5. The measurement of near-magnetic field has been performed by our project partner at IZM [5]. The *Hx* and *Hy* contributions to the magnetic field have been measured separately using appropriate probes.

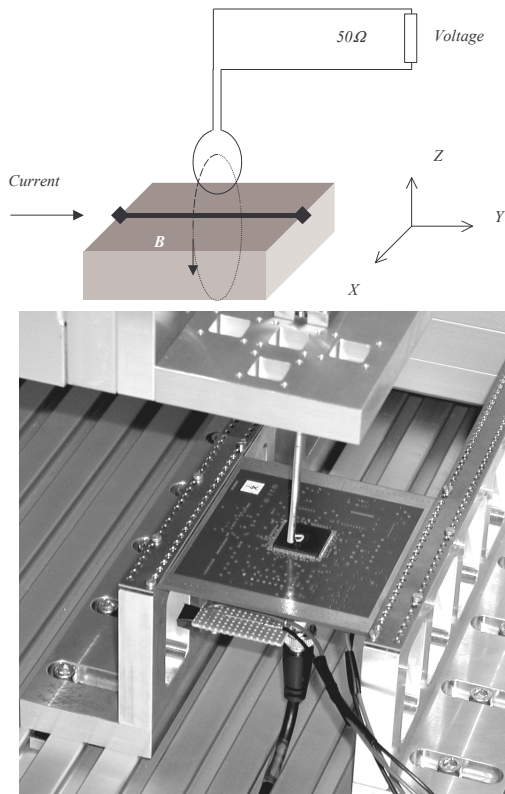


Figure 5. Principles for near field scan of the magnetic field

On the other hand, the CESAME test pinout chip has been described in an IBIS format [6], with details on the package parasitic R,L,C. In parallel, the electrical model of the core and supply network is given by the ICEM model, as described earlier in figure xxx. The analog simulation is performed by a Windows SPICE [7], while the Fourier Transform, current dipole magnetic prediction and user's interface is embedded in a specific freeware tool IC-EMIT [8] operating in Windows™ environment.

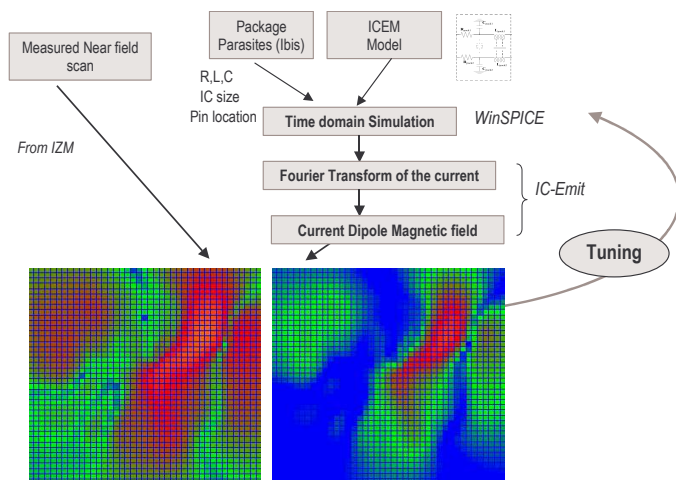


Figure 6. Figure 6: Proposed methodology to compare measured and simulated near field

The key idea of the magnetic field simulation is to consider the CESAME circuit as a set of current dipoles. Each dipole is associated to each package lead inductance. This means that in first approximation, each core of the CESAME test chip may be represented by two dipoles, one for the VDD current, one for the VSS current. The current flowing inside the IC itself is neglected. Only remains the lead current.

```

|
[Package model] qfp
|pack_width=20e-3
|pack_height=20e-3
|ic_width= 2.7e-3
|ic_height= 2.5e-3
|pack_pitch=0.5e-3
|ic_altitude = 0.8e-3

```

TABLE I. PHYSICAL PARAMETERS ADDED TO THE IBIS MODEL OF CESAME TO ACCOUNT FOR THE PACKAGE AND DIE SIZE

The package and die size information text are added in the [package model] section, in the IBIS file. The comment is mandatory to avoid parsing errors with conventional IBIS readers. However, IC-EMIT can locate 'pack\_' and 'ic\_' keywords and get the relevant information.

The magnetic field generated by of each elementary current dipole is calculated from the well know formation reported in figure 7, where  $l$  is the length of the current dipole,  $I_0$  is the current amplitude in the dipole (A), and  $\omega=2\pi.f$  (rad/s).

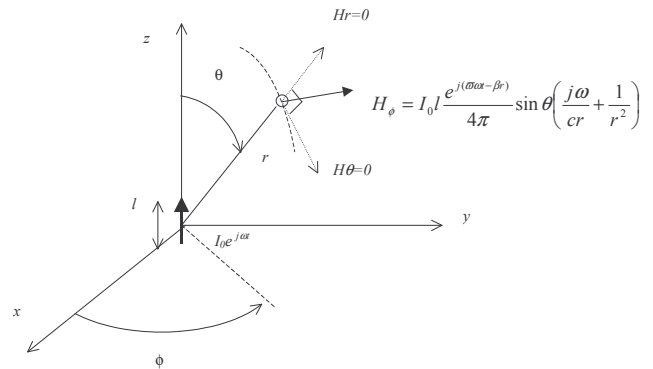


Figure 7. The magnetic field from an elementary dipole

The formulation of the magnetic field is only valid if the dipole length is much shorter that the distance  $r$  to the observation point. As the scan was performed at the altitude of 2mm, the current dipole length is set to 500μm. Each lead of the package is split into elementary dipoles as shown in figure 8. The software code has first been prototyped and validated under Scilab [8], and compared with a full 3D field solver [9].

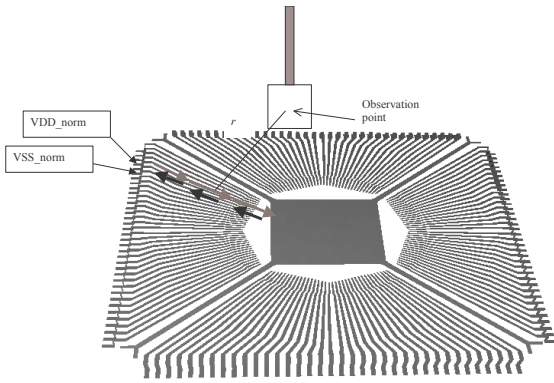


Figure 8. Each lead is considered as a series of elementary dipoles

A very good agreement between these results has been obtained in canonical situations such as one single current dipole.

The magnetic current at the observation point is the sum (in complex domain) of all elementary currents flowing in the VDD and VSS leads of the package. As VDD and VSS wires are routed very close, the magnetic field tends to cancel at a certain distance above the surface of the integrated circuit. An adaptation of the formulation to our practical case is required as the current is not a pure sinusoidal wave as for the theory, but a pulse (Figure 9), which gives a reasonable approximation of the real on-chip current.

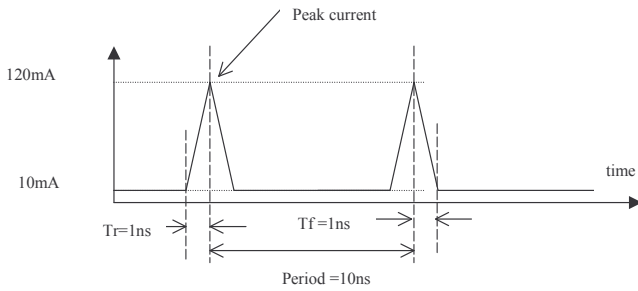


Figure 9. The approximated current pulse used in the ICEM model of the NORM and RC Core

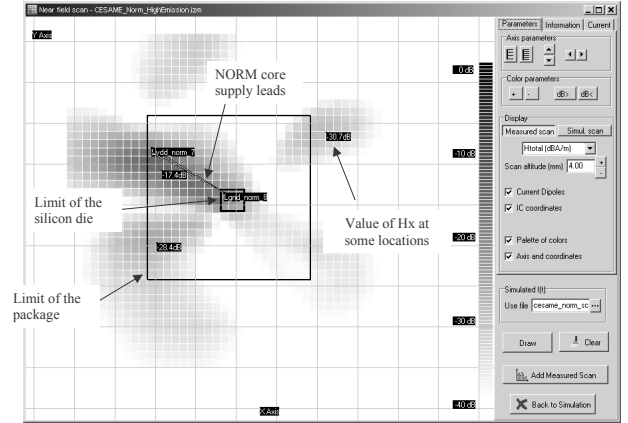
#### IV. RESULTS

##### A. SPICE Simulation Results

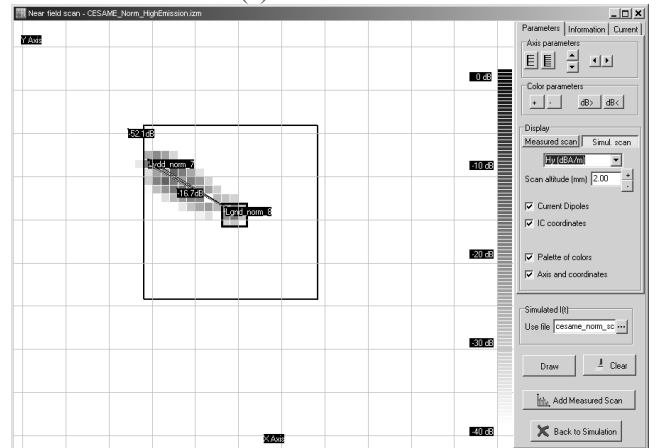
The SPICE simulation is performed in time domain in order to monitor all currents flowing in all inductances. For each current  $I(t)$ , a Fast Fourier Transform is performed to extract the current amplitude  $I\omega$  to be injected in the dipole equation, at a given pulse  $\omega$ . In the case of the NORM core, the IC-Emit user interface shown in figure 10 displays the position of the die, the package, and the position of the two main current dipoles. The SPICE simulation result is reported in the upper right corner of the window. It can be seen that VSS and VDD

are not exactly equal, which has been confirmed by on-chip sampling [5]. At 100MHz, the current amplitudes are 4.6 mA for VDD and 22 mA for VSS.

The measurement of the magnetic field has been performed on the CESAME test chip by A. Tankielun [5]. The  $H_x$  contribution of the magnetic field measured at 2mm above the ground plane is shown in figure 10-a. The peak magnetic field is  $-17\text{dB}$  near the main dipole. Three other regions exhibit magnetic field around 20dB lower than the main region.



(a) Measurement



(b) Simulation

Figure 10. The measured and simulated magnetic field  $H_x$  for CESAME NORM core

The distance between the measurement plane and the package lead-frame is estimated around 1mm. Consequently, the current dipole length has been set to 500 $\mu\text{m}$ , according to the assumption that the current dipole length should be smaller than the observation distance.

##### B. Two Dipole Radiation Results

The simulated magnetic field at an altitude of 2mm above the board surface is reported in figure 10-b. It can be seen that the

energy is only distributed among the package lead, as expected. The peak magnetic amplitude is  $-17\text{dB}$ . Decreasing the elementary dipole length to  $100\mu\text{m}$  do not change significantly the simulation and the peak magnetic field.

### C. Multiple Return path model

It has been proven that the return path of the ground current is not only the VSS pin of the core but also the other VSS connections of other cores, due to a common substrate. The coupling via the substrate is considered in the model shown in figure 11 as a resistance, which has be characterized in DC to a value of  $30\text{ Ohm}$ . The three inductance path correspond to the three core sharing the silicon bulk, weakly coupled to ground.

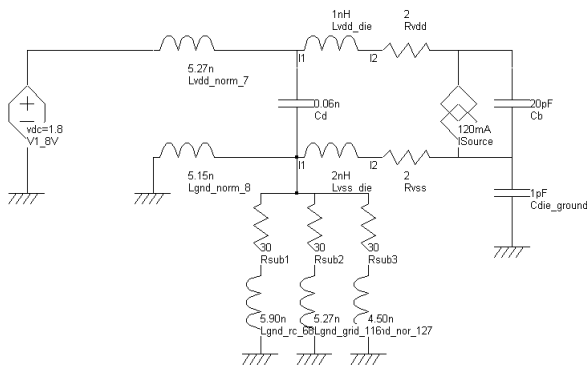


Figure 11. The multiple return path for the current due ti the share substrate

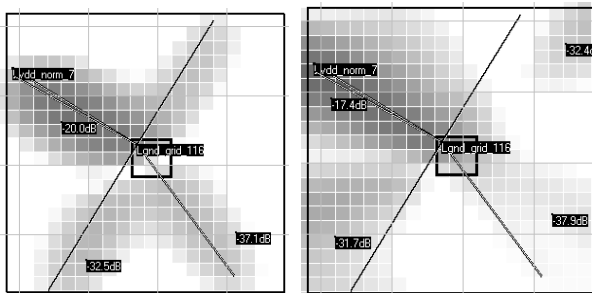


Figure 12. The simulated (left) and measured (right) magnetic emission of the NORM core in CESAME test chip

The simulation starts to behave closer to the measurements, as shown in figure 12. The simulation is based on one VDD

current dipole and four VSS current dipoles. The magnetic field appears above each lead, which is somehow what we measure on the surface of the IC (Figure 12-right). However, the energy is not exactly located at the position corresponding to the VSS leads.

Similar comparisons have been made for the RC core, with a good agreement using the multipole approach for the return current, which gives confidence in the ability of the approach to forecast the magnetic field generated by internal core switching at a short distance over the surface of the integrated circuit.

From these results, we hope to build a methodology for predicting the near-field electromagnetic compatibility of integrated circuits placed in highly integrated packaging such as system-on-chip.

### REFERENCES

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- [7] A Windows version of Berkeley SPICE is available at [www.winspice.com](http://www.winspice.com)
- [8] The SCILAB software may be download from <http://scilabsoft.inria.fr/>
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