Line geometry implications on crosstalk noise minimization

M.Roca[1], E. Isern[1], F. Moll[2]

[1]Departament de Física. Universitat Illes Balears, SPAIN
[2]Departament d'Enginyeria Electrònica, Universitat Politècnica de Catalunya, SPAIN

Abstract

In this work the different approaches to avoid crosstalk noise in VLSI integrated circuits are presented. The geometry of the cross-section of the lines is one of the more important parameters which must be considered when crosstalk problems are analyzed. Thus depending on this parameter we can select the best rule to avoid signal integrity problems in VLSI circuits. Several structures will be presented in this work in order to demonstrate the efficiency of the rules presented. The work is based on electromagnetic simulations to obtain the parasitic parameters, and HSPICE simulations using advanced CMOS technology models and very accurate distributed line models.

1. Introduction

Scaling down trend in microelectronic technologies implies an increase of parasitic coupling between interconnect lines. This effect causes unwanted signal integrity problems known as crosstalk noise [1,2]. Crosstalk can be shown to produce two main effects. The first one consists of the appearance of a glitch in a line which is in its steady state when a coupled line makes a transition [3]. The second effect, a change in the signal delay, is produced when both lines makes a simultaneous transition [4]. Crosstalk phenomena is expected to be an important concern in very deep submicron circuits. This fact has motivated research from different points of view, such as modeling and simulation [5], testing issues [6], experimental characterization [7], power issues [8] and design rules development. Regarding the last topic, different approaches can be considered. The circuit designer could detect the crosstalk effects using spice-like simulators when the layout is designed, and before circuit implementation. The designer may also follow several design rules developed for the sake of preventing or minimizing crosstalk noise. Otherwise, the designer could introduce additional lines, usually connected to ground, in order to introduce some shielding and hence minimize crosstalk effects. This work deals with the analysis of how the different design rules that can be used to reduce crosstalk noise depend on the geometry of the cross-section of the coupled lines.

2. Minimizing crosstalk

In this paper we analyze the efficiency of different rules to avoid or minimize crosstalk, depending on the cross-section dimensions of the lines. It seems quite obvious that the different parasitic parameters that characterizes the crosstalk noise (such as capacitance interconnect matrix, inductance interconnect matrix and resistance interconnect matrix or even conductance conductance matrix in sophisticated models) largely depend on the cross-section geometry of the lines.

The cross-section of lines evolves along with the technology. Although the actual quotient between the width and the height of the lines is very technology dependent, it may be pointed out a tendency for this quotient to decrease. That is to say, in current technologies line width scales more drastically than line height, and this tendency is expected to persist in future technologies. All in all, the methodologies to avoid or minimize crosstalk effects is going to depend on the technology, and in a certain technology on the width of the lines.

In this work a parameter α is defined as the quotient between the vertical dimension and horizontal dimension of a metal line. Thus, large α values will imply an advanced technology, whereas smaller α values are expected in well mature technologies. Nevertheless, it should be noted that for a given technology lines with different α values can coexist, because the designer can decide to make a wider line to minimize its resistance or prevent it from electromigration. The main objective of this paper is to discuss the effectiveness of different schemes in minimizing crosstalk depending on the value of the α parameter of the coupled lines.

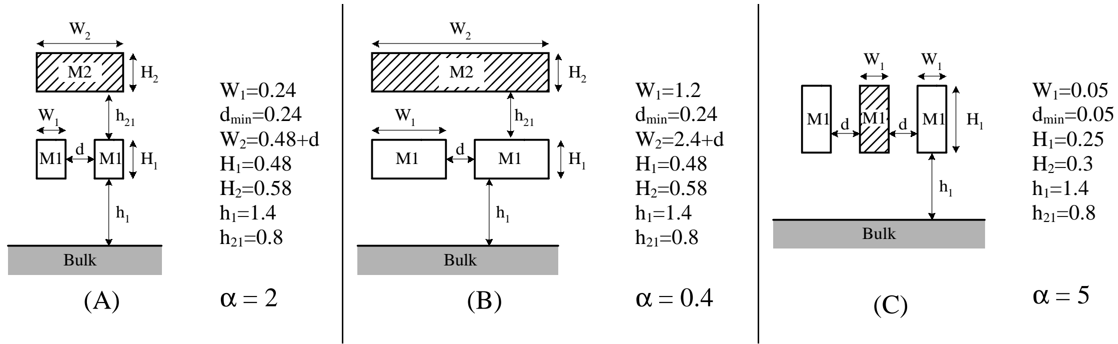

Figure 1. Three structures with different values of α. A modern technology with minimum size lines (A). A modern technology with wider lines (B). A possible future technology (C). Dimensions in μm.

3. Simulation and Results

The structures considered in this work are presented in Figure 1. The first structure (Figure 1.A) is composed by two coupled lines on a silicon substrate in a typical 0.18μm technology. For this structure we have $\alpha = 2$ and it will be used as an example of a current technology with minimum size lines. Two strategies to reduce crosstalk induced noise will be simulated and compared: increasing the spacing between metals (referred as SPA technique henceforth), and adding a shielding ground line in an immediate upper metal layer (referred as UPP technique).

The second structure (Figure 1.B) is intended to illustrate a case with smaller value of α. It may represent minimum size lines in an old technology or a modern one where the lines are wider in order to minimize the line resistance. The proposed structure presents $\alpha = 0.4$. The same two techniques to reduce crosstalk described for the previous structure will also be used in this one.

Finally, in Figure 1.C an structure with $\alpha = 5$ is illustrated. It corresponds to an extrapolation of current cross-section dimensions for a possible future nanometric technology. Due to the particular geometry of the lines (5 time higher than wide) increasing the spacing between metals (SPA) or even inserting a ground line in between (INS) are two minimizing crosstalk strategies that can be used without much area overhead penalty.

An analysis of interlayer dielectric thickness for several technologies in the last five years has shown that field oxide thickness does not scale as aggressively as metal thickness and intermetal spacing, even remaining practically constant in some cases. This have motivated the consideration of constant interlayer thickness for the 3 analyzed structures.

To derive the parameters that characterizes the behavior of the coupled conductors and electromagnetic field solver integrated in HSPICE have been used [9]. From the description of the 2-dimensional geometry of the structure the field solver provides a RLC matrix description of the coupling, which can be used as input to run an electric simulation of coupled transmission lines. This approach provides important advantages in front of using other field solver tools, as for example RAPHAEL [10], since the results can be directly introduced in the electric simulator, allowing the consideration of both an advanced transmission line model and accurate semiconductor devices models.

The circuit configuration used to analyze the coupled lines is depicted in Figure 2. Two CMOS drivers, which consists of CMOS inverters, are used to drive two coupled lines of length 100 μm, which are feeding two minimum size inverters. The inverter labeled "culprit" is dimensioned to have 10 times more driving capability than the inverter labeled "victim". An input transition with t_r = 200ps is applied to the input of inverter "culprit" whereas the input of inverter "victim" is held to a logic "1" value. An spurious glitch is expected to appear on the victim line due to the coupling. The height of this glitch ΔV will be used to quantify the crosstalk effect.

For this circuit and the 3 line topologies of Figure 1 HSPICE simulations have been conducted, using a level 49 model for the MOSFET devices, and a supply voltage of V_{DD} = 1.8 V.

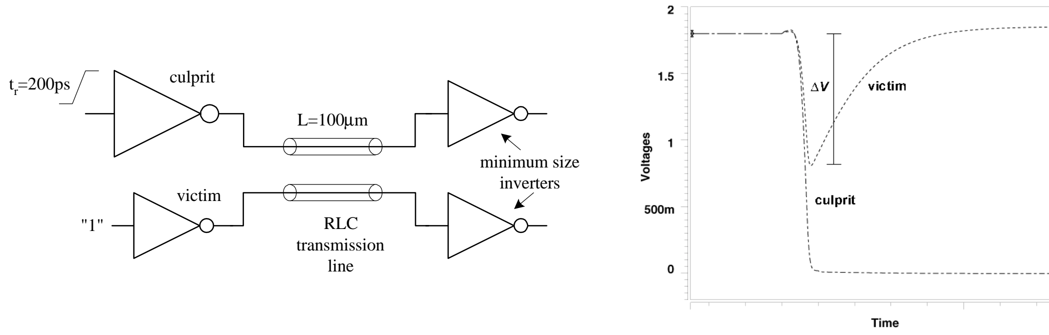

Figure 2. Schematic of the circuit used to analyze crosstalk. The effect of the transition of the culprit line when the victim line is at a fixed logic value is characterized by ΔV.

3.1 Case α = 2: modern technology

Figure 3 shows an HSPICE simulation for the two coupled lines geometry depicted in Figure 1.A. The capacitance and inductance matrixes provided by the field solver tool integrated in HSPICE are also shown. Along with the original two coupled lines (a), results are shown for three crosstalk minimization techniques: (b) spacing out the lines (SPA), (c) adding a ground line in the immediate upper metal layer (UPP), and (d) combining both techniques.

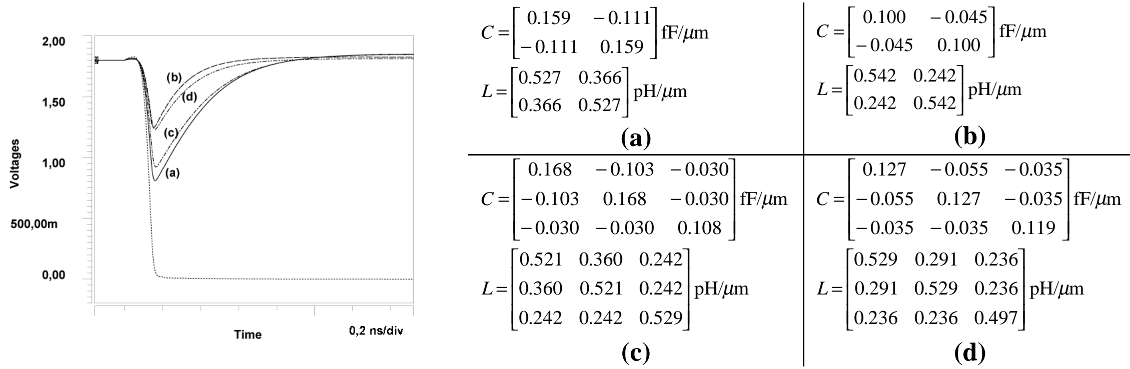

Figure 3. Crosstalk induced glitch for a line geometry with α = 2. Capacitance and inductance matrixes when (a) there is minimal space between lines, (b) SPA technique with $d=2d_{min}$, (c) UPP technique with $d=d_{min}$, and (d) SPA + UPP techniques with $d=2d_{min}$.

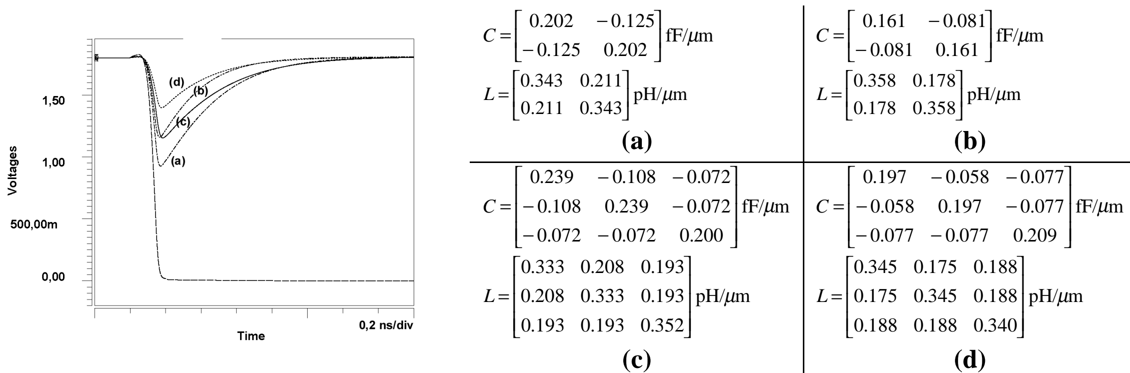

Figure 4. Crosstalk induced glitch for a line geometry with α = 0.4. Capacitance and inductance matrixes when (a) there is minimal space between lines, (b) SPA technique with $d=2d_{min}$, (c) UPP technique with $d=d_{min}$, and (d) SPA + UPP techniques with $d=2d_{min}$.

3.2 Case α = 0.4: wide lines in a modern technology

Figure 4 shows an HSPICE simulation for the two coupled lines geometry depicted in Figure 1.B. The capacitance and inductance matrixes provided by HSPICE are also specified. Results are shown for (a) the two original coupled lines, (b) spacing out the lines (SPA), (c) adding a ground line in the immediate upper metal layer (UPP), and (d) combining both techniques.

3.3 Case α = 5: possible advanced technology

Figure 5 presents an HSPICE simulation for the two coupled lines geometry depicted in Figure 1.C. As in the previous cases, capacitance and inductance matrixes are shown. The simulations corresponds to (a) the two original coupled lines, (b) spacing out the lines (SPA),and (c) inserting a ground line in between them (INS).

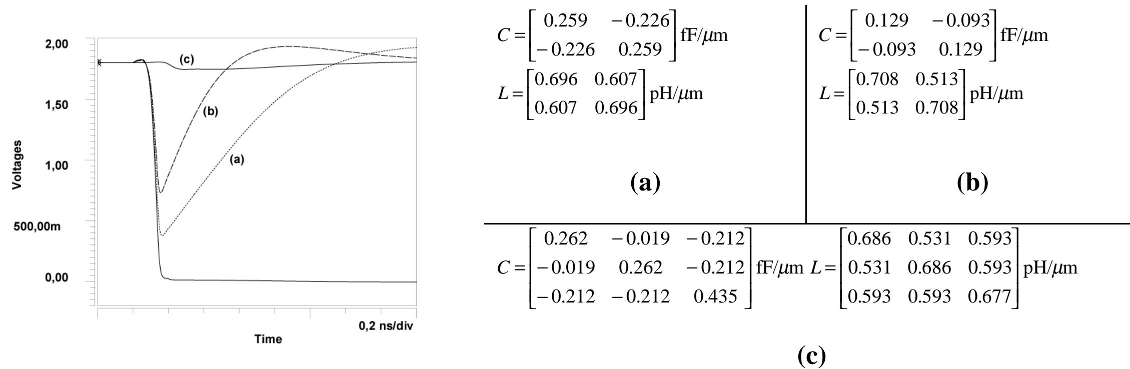

Figure 5. Crosstalk induced glitch for a line geometry with α = 5. Capacitance and inductance matrixes when (a) there is minimal space between lines, (b) SPA technique with $d=3d_{min}$, (c) INS technique with $d=d_{min}$.

4 Discussion and conclusions

From the results shown in the previous section, it is clear that different alternatives to reduce crosstalk effects should be applied depending on the value of α. That way, it turns out that in modern technologies, and when minimum width lines are concerned, enlarging the space between lines is the most efficient way to reduce crosstalk. If wider lines are involved, then the combination of spacing out and shielding with a ground line of an immediate upper layer metal should be preferred. Finally, it may be foresee that if current trend of α reduction is maintained in future technologies, then the solution of introducing a shielding ground line in between the two coupled lines will be the best option, both in terms of crosstalk minimization and area overhead.

Further research should be conducted on how the analyzed crosstalk reduction techniques may affect the dynamic behavior of the coupled lines (for example, their delay or input and fall time). That way, it may happen that a trade-off between crosstalk reduction and preservation of the dynamic parameters have to be considered when deciding how crosstalk minimization is take on. Finally, the efficacy of the proposed methods to reduce crosstalk effects concerning not only the spurious glitch but also the change in the delay of the victim line is an aspect the engineer must take into account to design crosstalk tolerant circuits.

5. References

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