

IBIS Models Quality: the Benefits of Frequency-Domain Analysis

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Abstract - A novel frequency-domain approach to digital buffer behavioural modeling is discussed. Although the IBIS specification has a very good potential, actual IBIS models underuse it, resulting in “low-quality” models. The aim of the presented method is to help modeling engineers in the production of “good-quality” IBIS models. Indications about the static components of the IBIS model (I-V tables and “C_comp”) are available through a quick analysis of the buffer impedance.

1 INTRODUCTION

The IBIS specification [1] has become the accepted standard for the behavioural modeling of digital buffers. Although the continuous development of the specification, the modeling potential of IBIS is often underused in the models actually available: there is a need for an improvement in the quality of the models produced.

In general, the IBIS models are created through time-domain simulations with the transistor model of the part to be modeled.

This work aims to highlight the contributions of a frequency-domain approach. The analysis of the buffer impedance vs. frequency gives clear indications about the quality of the static part of an IBIS model.

The explanation of the method leads to the analysis of some features about the behavioural modeling, concerning the die-capacitance and the differential resistance of a digital buffer.

2 THE IMPEDANCE OF AN IBIS MODEL

The IBIS specification [1] defines a capacitive parameter, C_comp, accounting for the effective parasitic capacitance between the buffer's pad and the power rails, on the die.

This capacitance is usually referred to with the term “die capacitance”.

In the IBIS topology, the buffer impedance is implicitly defined by the non-linear resistance resulting from the aggregation of the I-V tables shunted to the constant-valued die-capacitance (C_comp), as represented in figure 1.

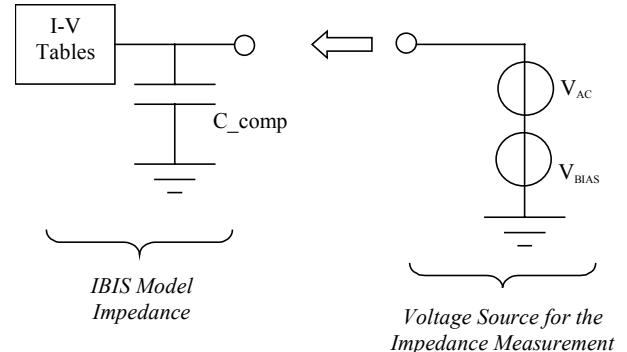


Figure 1: The model of the impedance implicit in IBIS, and the test set-up to measure the impedance in frequency-domain.

2.1 Frequency-domain analysis of the impedance of a digital buffer

Typically, the creation of an IBIS model is carried out through time-domain simulations on the transistor-level model. Advantages could be gained using a frequency-domain analysis approach, in particular in the two following areas of the modeling task :

- the determination of the C_comp parameter;

- the quality verification of the I-V tables data, resulting from the decimating algorithm.

Both these features concern the impedance of the buffer, and they apply to the modeling of any type of buffer (input, output, I/O,...).

The setup to run a frequency domain analysis of the impedance is shown in figure 1. The buffer node is attached with an AC-voltage source to test its impedance in small-signal regime, at various DC bias levels.

In figure 2 is an example of some impedance plots, at various bias levels, for a 5-Volt CMOS digital driver in the HIGH state. The solid line is the impedance obtained from the transistor-level model of the device; the dashed line is the impedance obtained from its IBIS model. It should be noticed that the IBIS model was generated from the transistor-model, which represents, then, the optimal reference term.

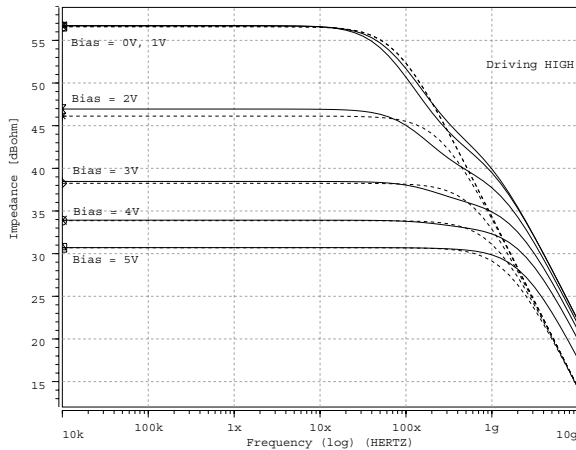


Figure 2: a 5-Volt CMOS buffer: impedance plots using the IBIS (dashed) and the transistor-level (solid) models, at various bias-levels.

Also, in figure 2 it can be noticed that at high frequencies the buffer impedance presents a "multiple poles" behaviour: as it will be better illustrated in the next section, a certain degree of incoherence is present between the IBIS and the transistor-model descriptions of the buffer's die-capacitance.

3 THE DIE-CAPACITANCE IN FREQUENCY-DOMAIN

From an AC-sweep on the transistor-level model, the small-signal impedance (Z_{buffer}) and/or admittance (Y_{buffer}) of the buffer is obtained.

The effective die-capacitance (C_{buffer}) of the buffer is then computed from the imaginary part of the admittance as

$$C_{buffer} = \frac{\text{Im}\{Y_{buffer}\}}{\omega}$$

The analysis on the previously used 5-Volt CMOS digital driver, reported in figures 3 and 4, show that the buffer capacitance is:

- non-linear (i.e., voltage dependent),
- frequency dependent,
- state dependent (high/low/high-Z).

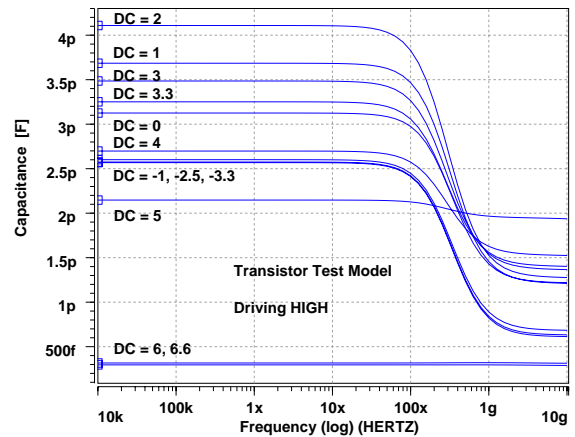


Figure 3: a 5-Volt CMOS buffer driving HIGH: capacitance vs. frequency, at various bias-levels.

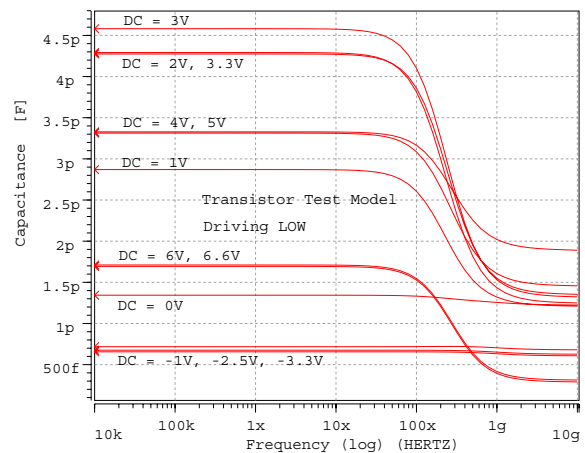


Figure 4: a 5-Volt CMOS buffer driving LOW: capacitance vs. frequency, at various bias-levels.

This features make clear that, unfortunately, the die-capacitance is not a univocally defined parameter [3]. The information contained in these images has to be translated in a *single constant value*, to be assigned to C_{comp} ^a.

^a In IBIS 4.0, ratified by the IBIS Open Forum in July 2002, the die-capacitance can be splitted in up to four constant parameters. The limitations described in the paragraph, apply also to this extension.

Also, the frequency dependency suggests that any time-domain method used for the determination of C_{comp} would suffer from a dependency over the spectral content of the time-domain function used as testing excitation (e.g., slope, period, ...).

However, the frequency plots of the impedance (figure 2), show how the choosen value of C_{comp} approximates the impedance of the original transistor-model.

4 QUALITY OF THE I-V TABLES DATA

The impedance plots (e.g., figure 2) show at low frequencies the differential resistance resulting from the aggregate of the I-V tables, at the given bias-level. The differential resistance is defined as

$$R_{diff}(V_{BLAS}) = \left. \frac{dV}{dI} \right|_{V_{BLAS}}$$

In a good quality IBIS model, the differential resistance resulting from the IBIS model should closely match the one resulting from the analysis with the transistor model.

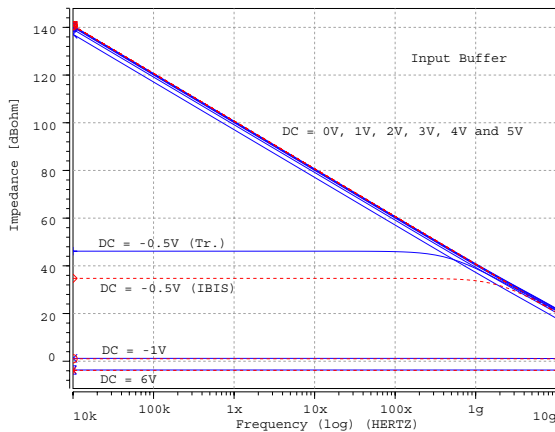


Figure 5: a 5-Volt CMOS input buffer – Impedance plots using the transistor-level (solid) and the IBIS (dashed) models.

For example, figure 5 shows a mismatch in the differential resistance between the transistor model and the IBIS model of an input buffer, at a bias level of -0.5 Volt. Further investigations lead to figures 6 and 7, where the differential resistance and the DC-current are plotted against the bias voltage, for both models. In particular, figure 7 clearly shows that the IBIS model clamps earlier than the transistor model.

In time-domain simulations, this can result in evident mismatches between the behaviour of an IBIS model and the original transistor model. As an example, the IBIS and transistor-level models in figure 5 have been compared in a time-domain simulation. A particular from the result is

shown in figure 8: a 43 mV mismatch appears, due to the early clamping of the IBIS model.

On the other hand, figures 6 and 7 show also clearly that not all the mismatches in the differential resistance, e.g. in the region between 0 Volt and -350 mV, would reflect in noticeable problems in a time-domain simulation.

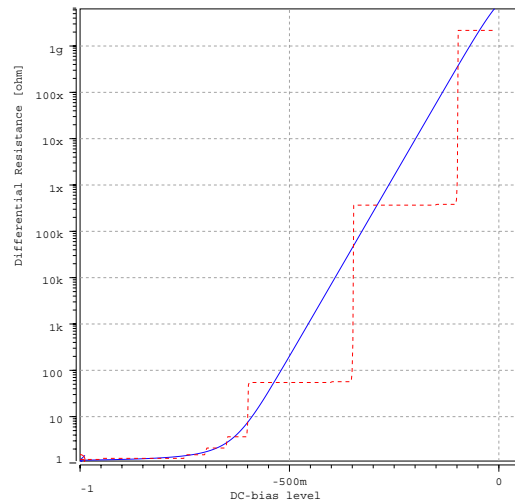


Figure 6: a 5-Volt CMOS input buffer - The differential resistance in the bias region $\{-1;0\}$ Volt – IBIS (dashed) and transistor-level (solid) models.

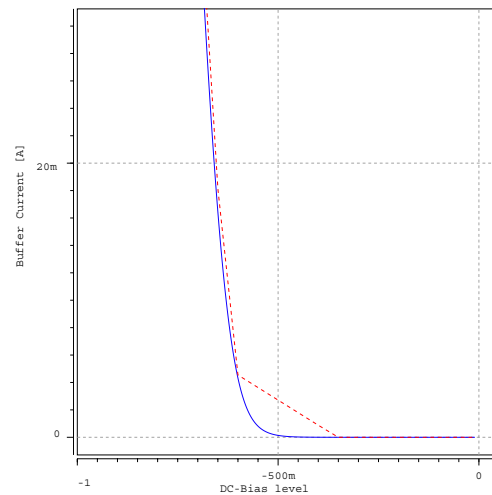


Figure 7: a 5-Volt CMOS input buffer – The buffer's DC-current in the bias region $\{-1;0\}$ Volt - IBIS (dashed) and transistor-level (solid) models.

Thus, a mismatch in the differential resistance should be seen as a *warning* about the model quality, and some further investigation should be conducted to confirm an eventual problem.

4.1 Typical origin of a low-quality I-V table

The generation of a good quality I-V table can be done in two steps. First, the transistor-level model is simulated with a very high degree of accuracy, i.e. the DC-current is measured for very small increments of the bias voltage.

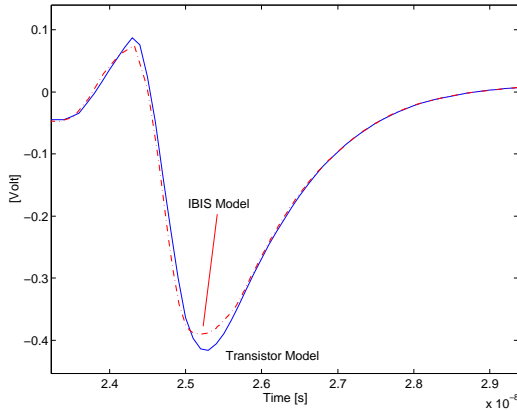


Figure 8: A time-domain mismatch due to the I-V tables' mismatch shown in figures 6 and 7: simulation using the IBIS (dash-dotted) and the transistor-level (solid) models.

In the second step, the table obtained previously has to be decimated. Various algorithm may accomplish this task. However, the common goal is to reduce the number of points to within the limit fixed by the specification (actually "100", as of IBIS 4.0), eliminating the table entries falling in the middle of the (almost) linear regions.

The first cause originating low quality I-V tables is the non-respect of the two steps approach previously outlined: often the I-V table is created with a single sweep of the bias voltage, using a constant increment. The result is a sloppy description of the I-V characteristic.

5 ACTUAL IBIS MODELS: AN EXAMPLE

Figure 9 is a typical example of the impedance plots obtainable with many of the actually available IBIS models. When compared to the reference model (i.e., the transistor-level model) of the same part, large mismatches in the differential resistance are clearly visible and the value of C_{comp} is, unequivocally, too low.

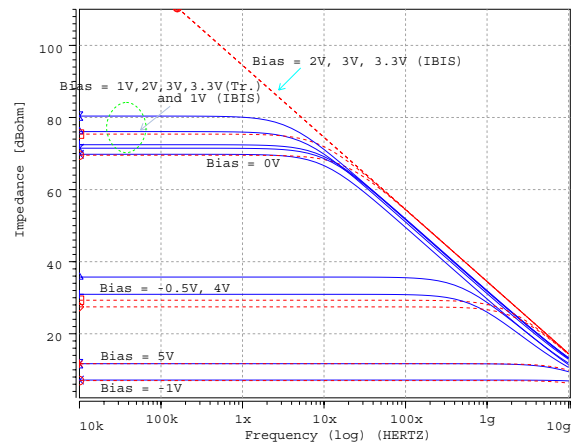


Figure 9: Impedance plots of 3.3-Volt INPUT buffer: a typical low-quality IBIS model (dashed), compared to the transistor-level model (solid).

6 CONCLUSIONS

A quick frequency-domain method to check the quality of an IBIS model has been described. The method considers the static part of the model: the I-V tables and the "C_comp" parameter.

The limits of C_{comp} in describing the die-capacitance have been analyzed and the notion of differential resistance of the buffer impedance has been discussed. A typical cause at the origin of low-quality I-V tables has been explained.

Finally, the method has been applied on a typical IBIS buffer, from a well-known IC-manufacturer, showing how important is the quality-problem in actually available IBIS models.

- [1] EIA-656-A, "I/O buffer Information Specification", Electronic Industries Alliance, edition 3.2, Sept. 1999.
- [2] Syed B. Huq, "Effective Signal Integrity Analysis using IBIS models", High-Performance System Design Conference, 2000.
- [3] L. Giacotto et al. , "Modeling the Non-Linear Reactance in Behavioural Digital Buffer Models", submitted to DATE'03, March 2003.