REGINA Test mask : Research on EMC Guidelines for INtegrated Automotive circuits

Christophe Lochot, Sébastien Calvet
MOTOROLA Semiconductor Products Sector, Digital DNA Laboratories
Le Mirail BP 1029, 31023 Toulouse Cedex France

Sonia Ben Dhia, Etienne Sicard
INSA-DGEI, 135 avenue de Rangueil, 31077 Toulouse Cedex 04 France

christophe.lochot@motorola.com, sebastien.calvet@motorola.com
Sonia.Bendhia@insa-tlse.fr, etienne.sicard@insa-tlse.fr

Abstract :

In this paper, the authors describe the part of the REGINA component that deals with the emissive behavior of the IC. The first part of this paper is a presentation of the different blocks that are useful to our experiments. The second part illustrates first measurements on this chip. We want to validate and/or create EMC design rules : with this test device we will be able to quantify the impact of each rule directly on the emission spectrum of the Integrated Circuit.

The REGINA test mask has been realized on the SmartMos7LV Motorola technology (0.35µm).

Introduction

To reach our objectives, we develop many elementary structures : a delay structure, a sensor on chip, and an emissive structure. Each structure is described below, and its functionality is illustrated with measurements. The test board we built to use REGINA offers a multiple configurations, especially for the power tracks (switches realized by short CMS resistances). In this paper, the chip has just one power supply. This test board was also designed to perform both radiated and conducted emission measurements [1], [2].

Delay structure

The delay structure (see Figure 1) was integrated in REGINA to desynchronize a signal and to monitor the time delay with the two Vanalog and Vplage voltage.

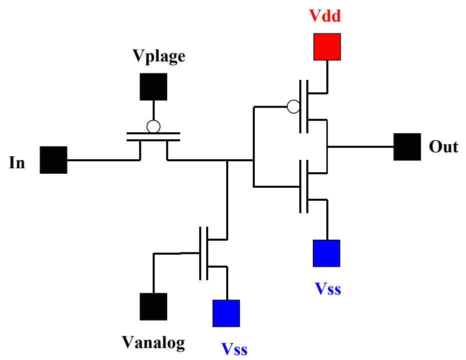

Figure 1 : Schematic of the delay structure

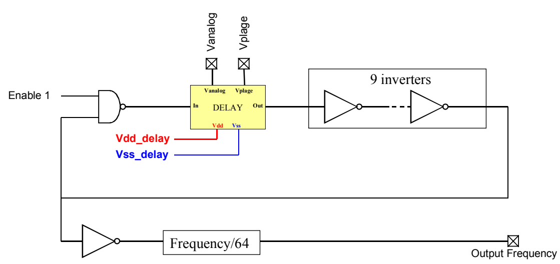

Figure 2 : Schematic of the delay calibration circuit

In order to calibrate our delay structure, we designed the calibration circuit illustrated in the Figure 2. The circuit is in fact a VCO, where the delay structure has been added. The oscillation can be observed on an external pad, after a 64-frequency divider for several values of Vanalog (Vplage is fixed), and is trigged with the input signal (enable1) coming from an external pad too. The delay calibration should be done for each component.

Sensor on chip

In order to see the internal currents, which are used in the ICEM model [6], we integrate in this specific chip a kind of on chip oscilloscope based on an on chip sample and hold circuit. The current is measured in fact through a specific resistance inserted in the supply track on the chip. Then, the sampled analog voltage is stored in a capacitance, before being amplified and exported out of the chip. The sampling cycle is repeated for a range of delays until the waveform is reconstructed (see Figure 3).

The sampling technique has been performed to have a 4-probes system on 2 output pads with an additional pad for the probes selection. The schematic of this sensor is given in the Figure 4 [4], [5].

The calibration of this sensor is still on going at this day.

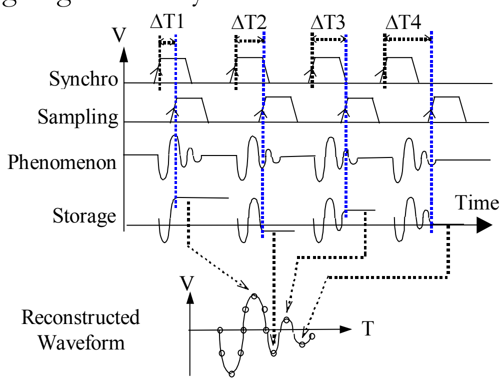

Figure 3 : Re-building of the observed data

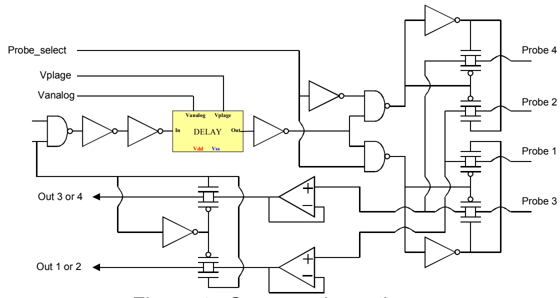

Figure 4 : Sensor schematic

Emissive structure

This structure is defined to generate current consumption on the supply line and to reproduce the behavior of a digital block. The amplitude of the current would be scalable (by monitoring the number of inverters which switch). Each inverters block could be delayed in a proportional ratio by using the delay structure. In fact, only the falling edge is delayed with this method (see the Figure 7). The schematic of this emissive structure is given on the Figure 5.

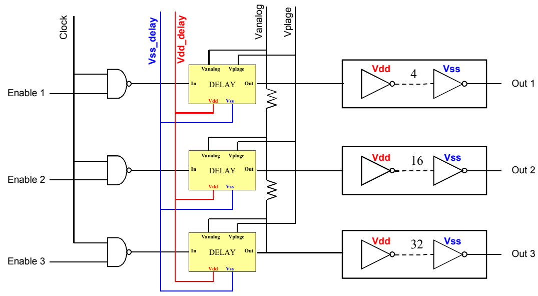

Figure 5 : Schematic of the emissive structure

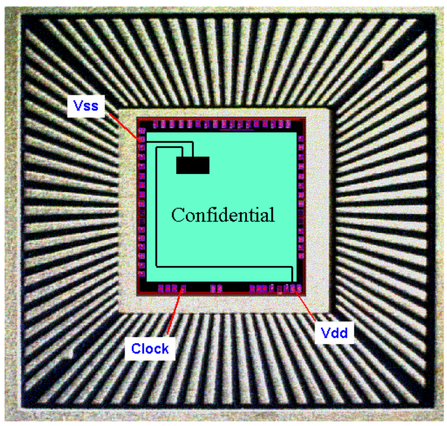

Figure 6 : Pinout of REGINA

Several emissive structures have been integrated in REGINA, each of them presenting a different power supply line. In The standard emissive structure is fed by 2 power tracks, which are coming from the opposite corner of the chip, as it is shown on the Figure 6. The small black box represents the standard emissive block that is used in the nest paragraph.

First Experiments

One of the first exploitation of this test chip is to see the influence of the digital signals synchronization on the power consumption. The experiment consists in adding a delay between the three inverter blocks of the emissive structure. The time curves of two blocks with delay are given on Figure 7.

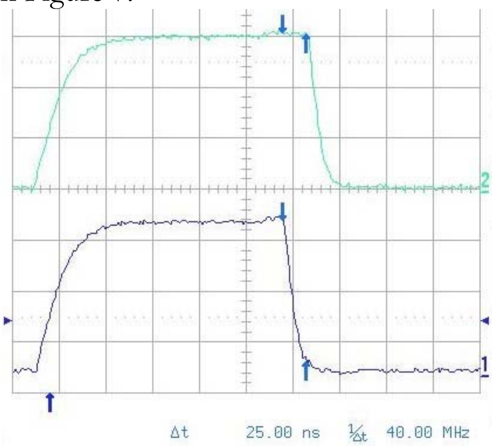

Figure 7 : Two Delayed Outputs

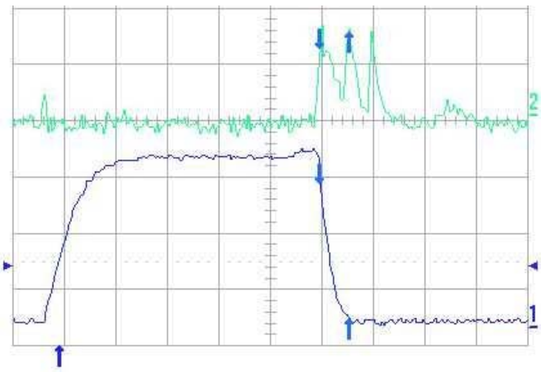

Figure 8 : Current measured on the 1 Ohm resistance

The current measured on the 1 Ohm resistance put on the Vss supply line is shown on Figure 8 .On the previous figure, we can observe the presence of three current peaks. They correspond to the switching of the three inverter blocks of our test mask.

If we compare the cases without delay and with delay (see Figure 9), we can conclude that a non-synchronous digital core will be less emissive than a synchronous one. Today, all the digital design flows are synchronous. Tomorrow, if we want to limit the emission of the digital core, we might have to look for new design tools.

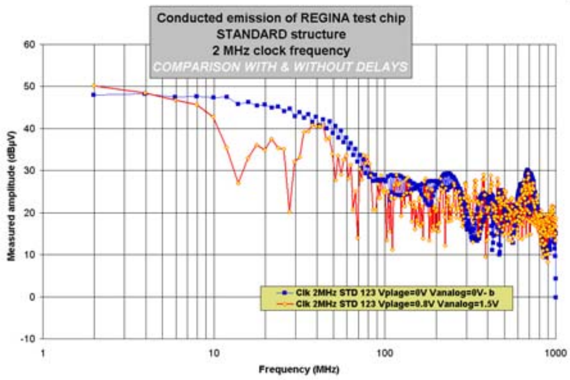

Figure 9 : Comparison with/without delay

Conclusion

In this paper, the authors presented the design of a specific test Chip for EMC research objectives. The different structures, delay, emissive have been validated. First measurements are encouraging and give some EMC design rule or trends. This test chip will provide internal measurement of the current that will then be used to validate the ICEM methodology. This will be a subject of the future paper in the next months. The authors integrated also in this pizza mask several structures in order to address the susceptibility of IC. A long measurement campaign is scheduled and should give a lot of interested measurements.

Bibliography

[1] IEC 61967-2 Integrated Circuits – Measurement of electromagnetic emissions, 150kHz to 1GHz – Part 2 : Measurements of radiated emissions-TEM Cell method

[2] IEC 61967-2 Integrated Circuits – Measurement of electromagnetic emissions, 150kHz to 1GHz – Part 4 : Measurement of Conducted Emission 1 Ohm /150 Ohms Method

[3] Modeling the radiated emission of microcontrollers, IBIS Summit Worcester, September 2001, Etienne Sicard, André Peyre-Lavigne, Christian Marot, Claude Huet

[4] INSA Thesis : Nouvelle méthodologie de caractérisation de l'intégrité de signal en technologie CMOS submicronique profond, November 1998, Sonia Delmas Ben Dhia.

[5] INSA Thesis : Mesure et modélisation prédictive des phénomènes parasites liés aux interconnexions dans les technologies CMOS, 1999, Fabrice Caignet

[6] IEC 62014-3 : Integrated Circuit Electrical Model (ICEM)

[7] Characterization of micro-controller electromagnetic emission : models for an international standard, S. Ben Dhia, S. Baffreau, S. Calvet, E. Siacard, Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, April 2002